MILLIMETER-WAVE AND TERAHERTZ INTEGRATED CIRCUITS FOR EXTREME ENVIRONMENTS

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MILLIMETER-WAVE AND TERAHERTZ INTEGRATED CIRCUITS FOR EXTREME ENVIRONMENTS

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of this research is to study the implementation of high frequency millimeter-wave (mmW) and Terahertz (THz) integrated circuits in silicon technologies for space applications. Several fully integrated circuits and sub-systems such as transceiver front-ends and array transmitters with on-chip phase-locked-loop (PLL) and antennas were implemented to show the possibility of realization of fully integrated THz circuits in SiGe technologies. Novel design techniques were implemented in these systems to enhance the performance of THz transmitter and receiver circuits. The reported circuits in this work were among the early realizations of Terahertz circuits in silicon technology and often achieved record performance metrics by utilizing novel circuit architectures and techniques. This includes the first report of fully integrated, fully phase-locked transceiver at THz frequencies. In addition, the effect of radiation intensive environments present in space was experimentally studied on mmW circuits for the first time. Novel methods to perform radiation experiments on high frequency circuits as well as modeling and simulation methodologies were proposed to understand the single-event effects (SEE) on high frequency receivers.

The following is the summary of the contributions of this work:

1. Investigation of single-event effects on W-band down-conversion mixers. W-band down conversion mixer was designed and implemented. Effects of single-event transients (SET) were investigated for the first time on mmW down-conversion mixer. Two-photon-absorption (TPA) laser experiment was conducted followed by device and circuit level simulations and analysis. This

work clarifies the propagation of the SET throughout the nonlinear switching circuit and identifies the sensitivities of this type of circuit to SETs [1].

2. Investigation of single-event effects on high frequency linear amplifiers. Several high frequency low noise amplifiers were designed and implemented. TPA laser experiments, as well as modeling, analysis and simulation of SETs on linear RF circuits were conducted in this study [2]–[6].
3. First study of SET effects on high frequency mmW receiver front-end. A novel methodology was proposed and implemented that enables the SET study of the receiver chain at high frequencies. Full W-band receiver as well as signal source and modulator was designed and implemented. TPA laser experiments were conducted, along with analysis, modeling, device and circuit level simulations [7]–[9].
4. Developing several mmW and THz signal sources, as well as fully integrated PLL at 117 GHz utilizing the novel technique of coupled VCOs for simultaneous power generation and distribution. The results of PLL work is under review in IEEE Journal of Solid-State Circuits, and the results of other signal sources were published in [10]–[12].
5. Investigation of the cryogenic operation of SiGe wideband LNA and devices [6], [13].
6. Developing novel phase-locking technique to synchronize free running signal sources to create higher power THz signals. A 2×2 network of signal sources radiating through on-chip antennas were implemented. The resultant power was combined in free space resulted in EIRP -0.3 dBm at 316 GHz [14]. The

extension of this work utilizing on-chip PLL and wideband antennas was designed and implemented at 230 GHz. This work demonstrates a fully phase-locked array system at 230 GHz with estimated EIRP of +10 dBm.

7. Collaborative research with members of SiGe team [15]–[19].
8. A novel sub-harmonic receiver as well as active antenna transmitter were developed which achieved record sensitivity at 314 GHz. Local-backside-etching was utilized to remove the silicon under the end-fire antennas for higher gain [12]. This work was extended to fully coherent transmitter and receiver with novel frequency doubler circuit and on-chip PLL. Two full transceiver front-ends with different receiver topologies were designed and implemented at 230 GHz. In addition, a fully integrated Transceiver / duplexer circuit was implemented at 117 GHz utilizing integrated D-band PLL.

CHAPTER 1. INTRODUCTION

The speed of silicon technology has increased steadily as a result of scaling and advanced device engineering over the last decades, enabling the realization of high-frequency millimeter-wave (mmW) and even sub-mmW integrated circuits (IC) in CMOS and SiGe technologies. mmW frequencies are referred to the frequency range where the free space wavelength of the signal becomes less than 10 millimeters, this band spans from 30 GHz to 300 GHz. Terahertz frequencies (THz) also known as sub-mmw frequencies are referred to a frequency range with less than a millimeter wavelength in free space. This frequency band spans from 300 GHz to 3 THz. There are numerous promising applications for high frequency communication, imaging, spectroscopy, chemical sensing and high-resolution radars in these frequency bands. There is also a growing interest in utilizing high frequency mmW radar, radiometry, and spectroscopy systems for space applications. Fully integrated solutions can significantly reduce the weight of electronic systems and make it perfect candidate for small satellites. However, the realization of integrated circuits in these frequency ranges remains challenging. In addition, the extreme environmental conditions in space with wide temperature variation and radiation intensive environment further increases the complexity of the design of these types of systems.

Compared to III-V technologies, which are commonly used for high frequency mmW and sub-mmW realizations, silicon has the advantage of higher yield and lower cost as well as the advantage of integration with digital CMOS.

The present study focuses on the implementation of high frequency circuit and systems operating at mmW and THz frequencies for space applications. Several Fully

integrated circuit and sub-systems were implemented and novel techniques were designed to face the challenges associated with the design, implementation and characterization of these types of high frequency circuits. Novel phase locking technique was proposed to synchronize on-chip signal sources without limiting the locking range of the coupled network. In addition, several techniques were proposed to improve the RF power generation at THz frequencies and to improve the sensitivity of THz receivers. Moreover, the effects of radiation intensive environments were studied for the first time on a full RF receiver. A novel technique was implemented which enables the SET testing of high frequency receivers. The effects of SETs were studied for the first time on RF circuits and full front-end receiver at mmW frequencies. The experimental studies were in close agreement with the developed models and simulation results. This study provides a framework to understand the SET effects on complicated systems such as RF front-ends, and to perform experiment and simulations on these types of circuits.

1.1 Silicon-Germanium Heterojunction Bipolar Transistor Technology

Bandgap engineered SiGe HBT devices demonstrate superior performance compared to silicon bipolar junction devices by adding a graded Ge to intrinsic base region of these devices. Although the concept of including Ge in silicon material backs to older days of the invention of transistor, it could only be implemented few decades ago with advances in manufacturing technologies. The SiGe HBT was first demonstrated in 1987 and commercialized in 1992. Inclusion of graded Ge across the base region creates an electrical drift field within the base region and impacts minority carrier transport. Thus, improves collector current density and current gain. In addition, the base and emitter transit times are also reduced by including graded Ge in the base region which directly results in

improvement of the f_T of the device. The details of physics of SiGe HBT devices can be found in [20].

SiGe HBT devices provide superior RF performance compared to CMOS devices while it can be integrated seamlessly in current CMOS technologies. Higher yield and reliability of these devices distinguish it from III-V technologies while offering lower cost. In addition, co-integration with CMOS devices allows the realization of high performance RF systems in a single chip with digital and analog CMOS circuits. Compared to CMOS devices however, SiGe HBTs can achieve similar f_T and f_{max} performance of more aggressively scaled CMOS devices. For instance, 130 nm SiGe BiCMOS technology can achieve similar f_T and f_{max} as of 45 nm CMOS technology. Thus, in terms of cost, SiGe BiCMOS technologies are even lower cost than CMOS counterparts with comparable RF performance. This also means that SiGe HBT devices will continue performance enhancement by further scaling, while CMOS devices are approaching the scaling limits. The current state-of-the art SiGe HBT devices achieve a 300 GHz and 500 GHz f_T and f_{max} respectively at room temperature. European DOTSEVEN project marches the path toward 700 GHz f_{max} in very near future [21]. With 700 GHz f_{max}, the realization of sub-mmW circuits with adequate power gain between 150 - 300 GHz becomes feasible. This improvement drastically enhances the performance of these types of sub-mmW circuits which are currently being implemented utilizing harmonic circuitries without amplification and with limited RF power. This technological enhancement can enable plethora of applications in sub-mmW frequencies in the next decade. Figure 1 shows the performance trend of current commercially available SiGe technologies.

SiGe HBT devices are thermally activated thus, demonstrate higher performance at lower temperatures with improved f_T / f_{max} and NF_{min} [22]. In addition, it is known that SiGe HBT devices are tolerant to multi-Mrads of total ionizing dose (TID) radiation effects. These unique features of SiGe HBTs make this device a perfect candidate for space applications.

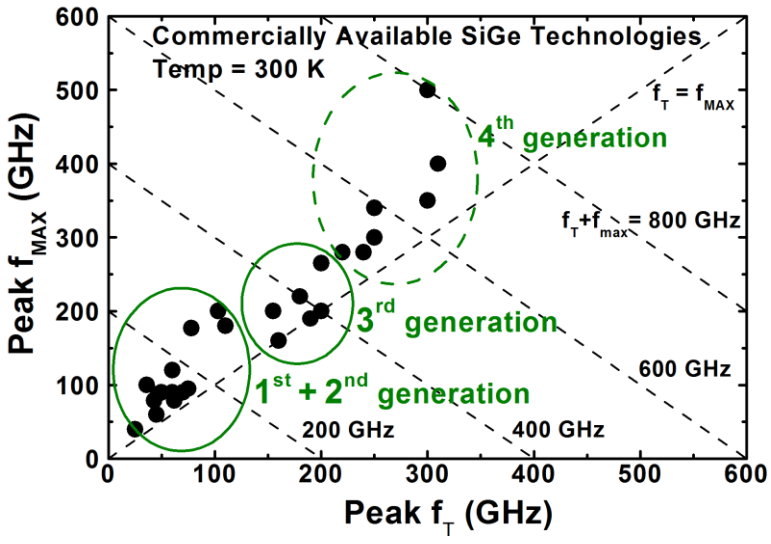

Figure 1. Peak f_{max} versus peak f_T of commercially-available SiGe BiCMOS technologies © 2013.

1.2 Millimeter-Wave and Terahertz Radio Design

The main bottleneck of the design of mmW and Terahertz circuits comes from the difficulty in generating high power and low noise signals as well as difficulty in designing low noise receivers. The free space path-loss is proportional to square of the frequency and rapidly increases by increasing the frequency. Therefore, the path loss is significantly higher at mmW and THz frequencies compared to lower frequencies, thus, the transmitter

signal is significantly attenuated before reaching the receiver. Figure 2 shows the atmospheric loss due to water and oxygen absorption across the frequencies. The atmospheric absorption is significantly higher at certain frequencies which are either resonance frequency of the oxygen or water. However, there are low-loss regions at mmW and THz frequencies that can be utilized for communication. The figure also shows that atmospheric absorption is smaller at higher altitudes.

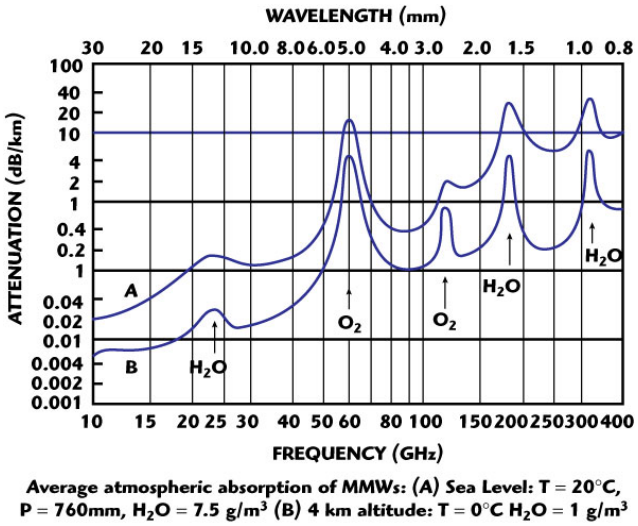

Figure 2. Atmospheric absorption of the RF signals in various frequencies.

The limited maximum available gain (MAG) of the transistors at sub-mmw frequencies, combined with higher NF_{min} of the devices, significantly limits the sensitivity of the receivers. Since, the transistors cannot provide power gain, most of the systems at Terahertz frequencies, do not employ LNA at the input of the receiver. Some receivers utilize detectors to directly convert the received RF power to DC voltage [23],[24]. The inherent nonlinearity of the detectors is utilized for this type of detection, where the input RF signal is mixed with itself when experiencing the quadratic function of the nonlinear device. This operation creates a DC component which is proportional to input RF power

and is used to detect the power of the incoming signal. These types of receivers are called non-coherent receivers and provide less sensitivity compared to coherent systems.

In coherent receivers, the received RF signal is mixed with an strong LO signal with a well-defined frequency to down-convert the incoming RF signal to an IF frequency [25]. The frequency of the resultant IF signal is the difference of the frequencies of LO and RF signals. This process is called down-conversion and is widely used in RF receivers. High gain and low noise IF amplifiers can now amplify the down-converted signal for further processing in digital domain after analog to digital conversion. Since the incoming small RF signal was multiplied by a large LO signal instead of mixing by itself, the output power of the coherent systems is higher than non-coherent systems. In addition, since the frequency of the coherent systems is exactly known, for narrow-band RF signals such as single tone RF signals, the IF bandwidth can be decreased significantly to increase the signal to noise ratio (SNR). This situation exists in imaging systems and Radars. Decreasing the IF bandwidth reduces the noise power without affecting the signal power, thus improving the signal to noise ratio significantly. Considering the low sensitivity of the THz receivers, a coherent system is highly preferred compared to non-coherent systems.

Coherent systems are standard approaches of low frequency high performance communication systems. However, these systems require well controlled LO signal, which is traditionally realized in the form of phase-locked-loop (PLL). Implementing PLL at mmW and Terahertz frequencies is extremely challenging. The limited power-gain of transistors, complexity of the circuit design at mmW frequencies, high frequency VCO and divider designs that can operate in a broad bandwidth, complexity of differential LO

distribution, as well as the low quality-factor of varactors limit the performance of these systems and increases the DC power consumption.

For high frequency mmW and THz systems which are the focus of the current research, providing a reasonably high-power RF signal is crucial. Due to absence of the front-end LNA in THz receivers, the sensitivity of the down-conversion mixer determines the sensitivity of the entire receiver. Inadequate LO power can significantly degrade the sensitivity of the mixers and receivers. Thus, providing a well-controlled and high power LO signal is necessary to improve the sensitivity of the receivers. At the transmitter side, the RF power directly impacts the performance of the communication link based on Friis formula. High-power RF signal combined with high gain antennas can compensate for the limited receiver sensitivity and high path-loss.

Generating RF power is the most challenging part of the design of THz systems. However, due to inadequate MAG in the current technologies, generating RF power is extremely challenging at mmW frequencies, while it is not even feasible at THz frequencies. The traditional approach to create THz signals utilizes the chain of frequency multipliers to generate RF power at THz frequencies [26]. Utilizing frequency multipliers allows the use of low frequency signal sources and relaxes its requirements in terms of phase noise and tuning range. Limited quality factor of varactors combined with resistive losses of the transistors, degrade the quality factor of the resonance tank and inversely affect the phase noise performance. Quality factor of the resonance tank directly impacts the phase noise of VCOs [27]. However, most of the reported frequency multiplier designs can only generate low output power while dissipating large amount of DC power [28], [29]. Some designs utilize amplifiers to effectively drive the frequency multipliers for higher

output power within the chain of frequency multipliers [28]. This approach can potentially generate more output power, but occupies a large layout area and consumes significant amount of DC power. In addition, for efficient power transfer, inter-stage matching networks are required and there is stability consideration in the case of any mismatch between the stages. Nevertheless, this approach is less desired for the implementation of arrays due to large DC consumption and layout area.

Some researchers use harmonic oscillators to create the frequency multiplication inside the VCO itself without additional circuitry. In this approach depending on the desired harmonic number, the effect of other spurious harmonics can automatically be cancelled while the desired harmonic is extracted. [30]–[34]. Despite having a compact size and lower DC consumption, this approach is unable to generate enough power at harmonic frequencies and requires additional amplification after signal generation which still suffers from the same problems as frequency-multiplication approach (increased size and DC consumption). Emerging various applications at THz frequencies however, has motivated the researchers recently to utilize harmonic oscillators with novel techniques for signal generation even beyond the f_T/f_{max} of the utilized technology. In [35] 3^{rd} harmonics of a 3-stage LC ring oscillator was extracted to generate a 482 GHz signal with -7 dBm output power in a 65nm CMOS technology. Since there are 3 stages in the loop with 120° phase shift, their 3^{rd} harmonic is combined constructively in the common node to provide stronger harmonic signal. Although this work reports promising results in creating high frequency signal source in silicon technology, but it still suffers from high phase noise and low output power as well as low power efficiency.

An elegant solution is to use arrays. In this approach, array of signal generators with limited output-power are combined to create more RF power. Figure 3 shows the block diagram of a system consists of array of several THz signal generators. A central signal source, feeds a network of amplifiers and frequency multipliers. Similar to frequency multiplier chains, the signal distribution network occupies a large layout area and consumes considerable DC power. In addition, due to large physical area, fitting the circuit components within the antenna elements becomes extremely challenging if not impossible.

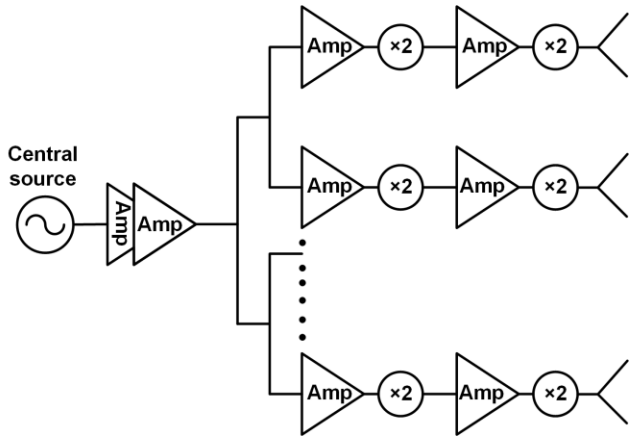

Figure 3. Block diagram of the transmitter array with a central signal source.

An alternative solution is to utilize local harmonic signal generators to minimize the area and DC consumption. The generated power from these sources are combined in free space to create more output power. These sources however, must have a same frequency and phase to combine constructively. Figure 4 shows the block diagram of this type of system. Injection-locking is a common technique to synchronize the signal sources, however the locking-range of this technique is limited.

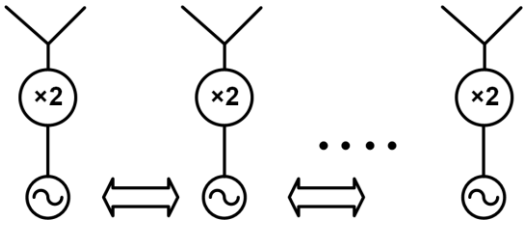

Figure 4. Block diagram of the THz radiating array with synchronized local signal sources.

In [36] a sub-harmonic coupling scheme was proposed to create a higher power phased array transmitter at 60 GHz. A similar approach was adopted in [33]. Four differential cross-coupled VCOs were coupled together in a loop with a controlling phase shifter in between the cells. By extracting 4^{th} harmonic of a signal at 80 GHz from each VCO, a 320 GHz source was realized that provides -3.3 dBm output power.

In [37], 16 signal generator units (4×4), were coupled together. The 4×4 signal generators were radiating and the resultant power was combined in free space to create +10 dBm of effective isotropically radiated power (EIRP). Each radiating unit is transmission line based oscillator which generates the signal and radiates at the same time. Injection-locking was utilized to lock the radiating units together utilizing an externally injected 47 GHz signal. A frequency tripler was utilized in each radiating unit to create 280 GHz signal. This signal is then used to phase-lock the radiating units utilizing injection-locking technique. The main drawback of this approach comes from the narrow locking-range of the injection-locking approach. In addition, each radiating unit utilizes a non-standard distributed oscillator to generate and radiate 2^{nd} harmonic content. Despite the possibility of multimodal operation, design for a certain frequency is challenging and may involve several simulations and try and errors.

In the present study, a novel method was proposed to locally lock the phase of radiating oscillator array in a loop configuration. The proposed technique creates strong coupling between the signal sources and operates only in a single mode. The locking-range of the proposed technique does not limit the operational bandwidth of the signal sources. In addition, the proposed technique can be applied to any standard oscillator topologies, and is extendable to any 2D array network. Details of this technique along with implementation results are addressed in CHAPTER 3. To lock the phase of the synchronized array system to an external stable reference, a PLL was implemented. The entire array was locked to the PLL which is locked to an external stable reference source. Therefore, the phase and frequency of the entire system was locked and controlled by PLL. The implemented PLL generates high power signals at 117 GHz with more than 10.8% locking-range and low phase noise. The circuit utilizes a novel technique of coupled VCOs for simultaneous signal generation and distribution within the feedback loop and output, thus a record output power of +8 dBm was obtained at D-band. CHAPTER 2 includes the details of this design and implementation results.

Sub-harmonic receiver is an alternative approach to mitigate the requirement of high frequency LO signal. A signal source with fraction of the LO frequency is required in this technique for frequency down-conversion. Thus, a lower frequency LO is utilized in these types of receivers without a need for frequency multiplication. Various types of sub-harmonic mixers have been utilized in low frequency receivers. One implementation scheme utilizes the nonlinearity of detector devices to down convert the incoming RF signal with the second harmonic of the LO signal [38]–[40]. This type of down-conversion experiences a large conversion loss and normally used in the receivers which includes high-

gain LNAs and is not suitable for the current design. In addition, a high power LO signal is required to achieve a reasonable conversion loss. Another architecture of the sub-harmonic mixer utilizes N-phase LO signals to switch multiple transistors ON and OFF within a single period of the LO signal. The process results in sub-harmonic down conversion. [41]–[43]. This approach is more compatible with the present system. In the present study, a novel sub-harmonic topology was proposed to effectively down-convert the incoming RF signal to lower IF frequency with minimal conversion loss. The receiver utilizes high power on-chip differential LO source and passive sub-harmonic type of mixer for frequency translation. Implementation results of a fully integrated 314 GHz transceiver with on-chip antennas is addressed in CHAPTER 4. In addition, two fully phase locked T/R modules were also implemented at 230 GHz with on-chip PLL. One receiver utilizes fundamental frequency down-conversion with on chip signal sources utilizing novel frequency doubler topology. Another receiver utilizes a sub-harmonic mixer for frequency translation similar to the 314 GHz receiver. Details of these designs and comparisons are addressed in CHAPTER 4. The last part of CHAPTER 4 describes the implementation results of fully integrated D-band (transmit-receive-multiplexer) TRX module which operates at 117 GHz and utilizes a D-band PLL. The high-power output of PLL was utilized for both transmitter and receiver to form a compact fully integrated transceiver.

1.3 Radiation Sensitivity of Millimeter-Wave RF Front-ends

There is a growing interest in utilizing millimeter-wave (mmW) frequencies (30-300 GHz) for satellite communications, space-based radars, radiometry, space exploratory probes, and landing systems. W-band radars are particularly interesting for cloud sensing

satellites [44]. The 94 GHz Cloud Sensing Profile Radar (CPR) instrument was used in the CLOUDSAT spacecraft, launched in 2006 [45], [46].

Because of the reduced wavelength at this high frequency range, mmW radar enables higher resolution for safe and precise landing on planetary bodies. Radar offers a superior solution for landing systems due to its ability to operate at any time of the day, weather and through dust and engine plumes, as well as its ability to detect velocity coherently [47].

High frequency mmW radiometers and radars have also recently been utilized in Cubesats for atmospheric sounding and scientific applications. Because of the extensive space-based applications, it is crucial to understand the behavior of these high frequency systems under the extreme environments present in space.

Electronic circuits experience more challenging conditions while operating in space. Radiation intensive environment along with wide temperature variations, bring new challenges to the design of robust electronics. SiGe HBTs are known to operate across a wide range of temperatures with improved performance down to very low temperatures [48]. Radiation intensive environment around the earth at the other hand significantly affects the operation of electronic circuits. Four different orbits have been recognized around the earth, each is subject to various particle source, type and intensities. Low earth orbit (LEO) which is considered below the altitude of 10000 km, medium earth orbit (MEO, between 10000 to 20000 km), geostationary orbit (GEO, at 36000km) and highly elliptical orbit (HEO).

Charged particles resulted from solar winds and cosmic rays in space are trapped by the magnetic field around the earth known as magnetosphere. These energetic charge particles form a radiation belt around the earth, which is known as Van Allen belts. These belts are composed of electrons, protons and heavy ions that traverse around the earth. Magnetosphere of earth protects human and other creatures from harmful charged particles and allow the life on earth. The charged particles trapped in Van Allen belts however, can have high energies and can significantly impact the orbital electronics. The electrons in Van Allen belt can possess energies up to 7 MeV. While proton energies can extend from several hundred MeV close to earth's atmosphere to a few MeV on the outer edges of Van Allen belts [49], [50]. The Van Allen belt around the north-eastern coast of south America is the closes to earth's atmosphere due to magnetic field depression on that area and causes detrimental effect for LEO satellites. Van Allen belts have dynamic radiation intensity which strongly depend on the solar cycle. The radiation belts of other planets might be significantly more intense than Van Allen belts. For instance, the magnetosphere of Jupiter has a million times the volume of earth's magnetosphere. Thus, Jupiter has more intense radiation belt.

The effects of radiation on electronic devices can be classified in three categories, total ionizing dose effect (TID), displacement damage (DD), and single event effects (SEE).

When a high energy charged particle strikes the device, energy of the particle is transferred to the material. This energy is dissipated either through elastic scattering or photon emission or electron-hole pair generation. Linear energy transfer function (LET), is used to describe the rate of energy loss in the material, which stands for the energy loss

of the particle for unit length traverse across the material, normalized to density of the material. The most common unit of this measure is $\frac{Mev.cm^2}{mg}$. LET is material dependent.

If the energy of the incident particle was very high, it can potentially displace an atom in the lattice, this phenomenon is called displacement damage. Which can cause extra leakage within the device, reduction in carrier mobility and increase in carrier tunneling across barrier [20]. In advanced semiconductor technologies, due to extremely small footprint of the active devices, and high background doping, DD effect is quite minimal and will not be addressed in the present research. The high energy particle can also damage the oxide interface and cause severe detrimental effect. In SiGe HBT devices however, the area of the oxide layer is much smaller than the device, thus SiGe devices are inherently tolerant to this type of damage. Charged particles and holes resulted from ionizing radiation exposure, however, can be trapped and accumulated in the oxide interface during the satellite mission and create interface charge traps in the oxide interface, thus increase the leakage currents. The added base leakage current reduces the device gain. This phenomenon is described as total ionizing dose effect and, since the SiGe devices have quite small oxide interface, (emitter-base spacer and shallow trench oxide) SiGe HBT devices are quite tolerant to TID effects up to multi Mrads. The increased base leakage current may impact low current devices, however since the RF circuits are normally biased at high current regime, the TID effect is negligible in the context of RF circuits. However, CMOS devices can be sensitive to this effect, since it slightly changes the threshold voltage and increases the leakage current. This phenomenon can be an issue for devices biased in very low biasing currents or sub-threshold region.

TID effect is mostly accumulated charge effect within the device oxide interface. Heavy ion strike on semiconductor devices can generate a highly dense track of electron hole pairs within the device, which is sometimes higher than background doping of the substrate of transistors. Thus, these charges diffuse to nearby PN junction of the device and since active devices are biased with strong electric fields across the device. These extra carriers are pulled out of the device and cause transient charge / current excursions. The generated carriers propagate within the circuit and can cause temporary transient voltage and current excursions in several circuit nodes or even can permanently damage the device. The former effect is called soft error, and the latter is called hard failure. This phenomenon is known as single event transient and is the focus of the current research. In logic circuits, such as flip-flops which store data bits, SET can cause bit flipping and loss of the data, which is known as single-event upset (SEU). In addition, a latch-up can occur by triggering the parasitic bipolar transistors within CMOS devices upon SET which can cause destructive damage by conducting a large current through the conducting channel of the CMOS device.

SiGe HBT devices are inherently tolerant to TID and DD, but they exhibit high sensitivity to SEEs. SEU was first observed during an above ground nuclear test at 1954 - 1957 where anomalies on electronic equipment were observed. The first anomalies in communication satellite operation were reported in 1975 [51]. The first destructive SEE, was the result of proton induced latch-up in memory of an instrument of the polar ERS-1 satellite. The failure had occurred over the South Atlantic Anomaly (SAA). Over the past recent decades considerable research has been conducted to understand and quantify the SEEs on microelectronic circuits.

The research in the present thesis, focuses on the understanding of the SEE effects on high frequency circuits.

Comprehensive studies have been done on the effect of SETs on various SiGe HBT technology nodes [48], [52]–[54]. Single-event transients have also been extensively studied in digital circuits, and radiation hardening techniques have been proposed [55]–[57]. However, only limited research on the effects of SETs on RF circuits have been conducted, with no study on the effect of SETs on more complicated electronic systems such as RF front-ends. The reported circuits are typically operating around a few GHz. SET on VCOs have been studied in [58], [59]. In [4] SETs on a 2.4 GHz LNA was studied and inverse mode operation as a radiation hardening technique was proposed. SET studies on a front-end switch was reported in [60].

In the present study, the sensitivity of a full mmW radar front-end to SETs was investigated. The effects of SETs were studied on various circuit components of the receiver. Theoretical and experimental studies as well as thorough modeling and simulations were conducted. A close agreement between the experimental data and simulation was achieved. The research presented in this thesis clarifies the effects of SETs on RF front-ends. In addition, a novel methodology was presented which allows the experimental study of the effects of SETs on high frequency RF and mmW systems. A modeling methodology was proposed for simulation purposes that follows the experiments very closely. These studies clarify the propagation of SET throughout a receiver chain, a study never accomplished before. The details of this study are documented in CHAPTER 5 and CHAPTER 6.

CHAPTER 2. D-BAND PHASE-LOCKED LOOP

2.1 Introduction

Short wavelength and the availability of the wide spectral bandwidth are the main advantages of mmW and THz frequencies. The short wavelength benefits high resolution radar and imaging systems. In addition, it enables the realization of integrated antennas for full integration of mmW systems, thereby eliminating the costly and challenging high frequency packaging. Automotive radar is an example of the most well-known mmW radar application [61]–[65]. Other types of high resolution radars at frequencies above 100 GHz utilizing CMOS and SiGe technologies have been reported in [66]–[70]. Weather monitoring radar systems and radiometers as well as high-speed communication systems are other examples of mmW circuits that can be implemented in silicon technology [7], [71]–[75].

Most of the above-mentioned systems require wideband and low noise timing circuits which are traditionally realized using frequency synthesizers. A synthesizer consists of a tunable-frequency voltage-controlled oscillator (VCO) which is controlled in a feedback loop. Integrated VCO is traditionally implemented utilizing a positive feedback which utilizes passive on-chip components for frequency selectivity. The phase noise and frequency stability of the VCOs, however, are related to the quality factor of the passive components. Unfortunately, the quality factor of the on-chip passive components is small, thus on-chip VCOs do not provide adequate frequency stability and the frequency of the VCO drifts over the time. A PLL locks the phase of the VCO signal to a stable low frequency oscillator, which is mainly built using high quality crystals. To establish such a

locking mechanism, a feedback loop is created that enforces the phase of the VCO to follow the phase of the low frequency stable crystal oscillator. Figure. 5 shows the conceptual block diagram of a general PLL architecture. A chain of frequency dividers, divide the output frequency of the VCO down to the frequency of the stable crystal oscillator. The phase of the frequency-divided signal is compared with the phase of the crystal oscillator to generate an error signal. The error signal tunes the oscillation frequency of the VCO. The negative feedback in the PLL architecture assures that error signal finally becomes zero (for PLLs with infinite loop gain such as charge-pump PLLs). The condition in which the phase of the frequency divided signal exactly follows the phase of the crystal oscillator and phase-locking occurs. Thus, the PLL loop achieves the frequency stability of the highly-stable crystal oscillator within the bandwidth of the feedback loop.

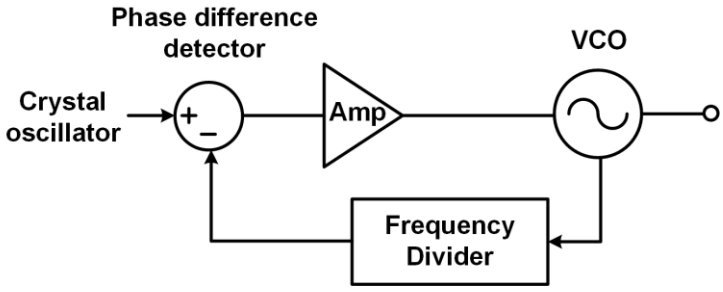

Figure. 5. Conceptual block diagram of a general PLL.

A synthesizer is special type of PLL in which the frequency dividers are programable. The output frequency of the PLL is the multiplication of the crystal frequency by the division ratio. Thus, the output frequency of the PLL can be programmed by programming the division ratio to synthesize various frequencies. Unfortunately, the implementation of high performance mmW synthesizers above 100 GHz is challenging. The limited power-gain of transistors, complexity of the circuit design at mmW frequencies, high frequency VCO and divider designs that can operate in a broad

bandwidth, complexity of differential LO distribution, as well as the low quality-factor of varactors limit the performance of these systems and increases the DC power consumption. Nevertheless, mmW synthesizers have been reported in SiGe and CMOS technologies. However, there are only a few fully-integrated examples of the synthesizer designs above 100 GHz in silicon technology. Most of these PLLs utilize low frequency PLLs followed by frequency multipliers [64],[67], [76] or extract the higher harmonics of a low frequency PLL [77]–[79]. Although frequency multipliers can potentially provide adequate power, the harmonic extraction techniques normally suffer from low output power. In [80], a higher frequency oscillator was injection-locked to harmonics of a lower frequency PLL to provide a locked signal at mmW frequencies. Similarly, a lower frequency PLL followed by injection-locked frequency-multiplier was proposed in [81]. The locking-range of these systems are typically limited because of the limited locking-range of the injection-locking technique with small injection power.

With increased speed of highly-scaled si-based technologies, the realization of high performance fundamental frequency PLL above 100 GHz has finally become feasible; however, to date there are only few reported fundamental frequency PLLs in silicon [82]–[84]. These designs all have narrow locking-range with small output power. By utilizing several design techniques, the proposed fundamental frequency PLL in the present design achieves wide locking-range and high output power.

LO routing and distribution is challenging at mmW frequencies. A large portion of DC consumption comes from the LO distribution network in mmW PLLs [77],[85]. Providing high power mmW signal, greatly simplifies the LO distribution network and can significantly reduce DC power consumption in mmW systems. Despite the required high

output power, considerable RF power is required to lock the frequency dividers in a broad bandwidth. In [85] one of the differential outputs of the VCO was taken for the output and the other was utilized to drive the frequency dividers where extra power dividers, amplifiers and baluns were incorporated in the LO distribution network within the PLL. In [77], 600 mW was consumed for the LO distribution network and multiplexing between two VCOs at different frequencies. The LO distribution network was consisted of several amplification stages within the PLL. Besides additional DC power consumption and die area, the amplifiers should provide wide bandwidth to cover the entire tuning range of the VCO. In [86], a triple-push VCO was utilized in which the 3rd harmonic was extracted for the output while the fundamental single-ended signal was utilized for injection locking with frequency divider. Despite the narrow locking-range of injection locking technique, particularly with single ended injection, the utilized triple-push topology was prone to common mode excitation and couldn't provide balanced signals neither for the output nor for the frequency dividers.

In the present design, we propose the use of coupled differential VCOs for simultaneous balanced power generation and division in mmW PLLs. The proposed technique utilizes direct, double-injection fundamental signal coupling methodology with high power and strong coupling throughout the entire tuning range of the VCOs. It provides separate high power balanced signals for the output and frequency dividers to assure wideband locking. Thus, the present design can generate more than +8 dBm output power into a 50 Ω load without additional amplification. The generated power can be used in transmitter without the need for additional PA, or it can be leveraged in LO distribution network to avoid additional amplifiers and buffers. The proposed architecture relaxes

differential LO routing, improves phase noise, increases the output power and enhances the locking-range of frequency dividers, all at the cost of increased DC consumption.

A PLL with more than 10% locking-range at 117 GHz was realized. The proposed PLL was implemented in 130 nm SiGe technology, provides more than +8 dBm of output power with better than -100 dBc/Hz and -121 dBc/Hz at 1 MHz and 10 MHz offset from 116 GHz carrier, respectively.

2.2 VCO Design and Coupled VCOs

Locking-range of the PLL is typically limited by the VCO, and therefore it is important to maximize the tuning-range of the VCO. In addition, the phase noise of the PLL is determined by the phase noise of the VCO at higher offset frequencies. The output power of the VCO is also critical in many applications, so that the number of power hungry LO drivers and amplifiers be minimized.

To satisfy the requirements of the VCO, both design and topology selection play important roles. It is known that the Colpitts topology has superior performance at millimeter-wave frequencies in terms of phase noise and tuning range [87], [10]. The phase noise superiority comes from the topological characteristics of this circuit, where the so-called impulse-sensitivity functions (ISFs) of the main transistors experience a minimum value during the conduction time [88]. In other words, the transistors in this topology conduct current in time instants when the sensitivity of the output phase to injected perturbation is minimum, and thus the noise contribution of these devices are reduced, resulting in better phase noise performance. The maximum achievable oscillation frequency of this topology is also greater than the commonly used cross-coupled topology,

which makes it a better choice for VCO designs at frequencies operating at a significant fraction of the f_{max} of the utilized process technology [89].

Equation 1 shows the well-known Leeson's formula for the phase noise of electrical oscillators [27]. The quality factor of the resonator (Q) and power of the generated signal (P_{sig}) are the two important parameters to reduce the phase noise of oscillators. At mmW frequencies, however, the Q of the resonator is mostly dominated by the Q of the varactors, and parasitic resistors of the transistors. Therefore, it is important to increase the Q of varactors and improve the overall phase noise of the circuit.

$$\boldsymbol{L(\Delta\omega) = 10\log\left(\frac{2K_BT}{P_{sig}}.\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)} \qquad (1)$$

ω_0 is oscillation frequency, T is temperature, K_B is the Boltzmann's coefficient and $\Delta\omega$ is the frequency offset from the carrier. With improved f_{max} of SiGe technologies, the base and emitter parasitic resistors have been reduced and the Q of the junctions has been improved, making the SiGe HBT suitable for use as a mmW varactor. Accumulation mode MOS (AMOS) varactors are another option that have been used in recent publications [77], [85]; however, due to higher achievable Q, we chose to utilize SiGe HBTs for the varactors for the current design. Figure 6 shows the schematic of the differential Colpitts VCO utilized in the present design.

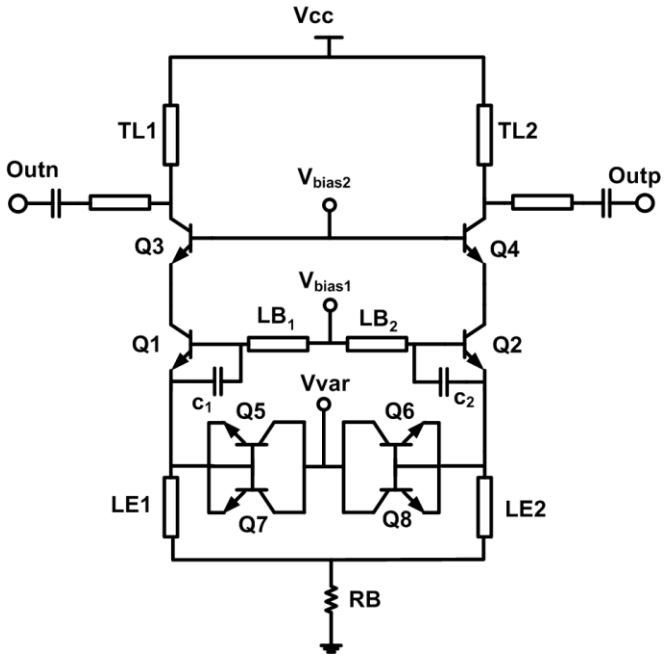

Figure 6. Differential Colpitts VCO with cascode buffer.

The layout of the varactors was carefully designed to minimize the impact of parasitics from interconnections, which can limit the tuning-range. Capacitors C1 and C2 were realized using MiM capacitors and the combination of these capacitors and via connections were EM-simulated using Sonnet software. These capacitors reduce the AM to PM conversion at the base-emitter junction, and reduce the noise from base resistance, thereby improving the phase noise. [90]

The peak amplitude , phase noise of the signal, and negative resistance of a generic Colpitts oscillator can be calculated using Equation 2-4. [91], [92].

$$A_{tank} = 2I_C R_T (1 - n) \qquad (2)$$

$$L_{ic+RT}(\Delta\omega) = 10\log\left(\frac{K_B T(1+n)}{4R_T n C^2 A_{tank}^2 \Delta\omega^2}\right) \quad (3)$$

$$R_{NEG} = \frac{-4\pi^2 g_m L_B (C_1 + C_\pi)}{(C_1 + C_\pi + C_{var})^2} \quad (4)$$

$$n = \frac{C_1 + C_\pi}{C_1 + C_\pi + C_{var}} \quad (5)$$

$$C = \frac{(C_1 + C_\pi)C_{var}}{C_1 + C_\pi + C_{var}} \quad (6)$$

$$\omega_0 = \frac{1}{\sqrt{L_B C}} \quad (7)$$

I_C is the biasing current, R_T is the equivalent tank impedance at the resonance frequency which is directly related to Q of the resonator tank, A_{tank} is the peak amplitude of the signal, g_m is the transconductance of Q1 SiGe HBT, C_π and C_{var} are the base-emitter junction capacitance and varactor capacitance respectively, and $\Delta\omega$ is the offset from the carrier frequency.

Equation 2-6 shows the dependence of VCO performance on several design parameters which makes the design of an optimized VCO challenging. The design methodology proposed in this work, provides a step by step procedure for the design of an optimized mmW Colpitts VCO. As opposed to low frequency designs, the design of present was started by designing the varactors first. The following steps outline the design procedure of the optimized mmW Colpitts VCO.

1) Design the varactors to obtain high Q and large $\frac{C_{max}}{C_{min}}$ ratio to satisfy the targeted tuning range. Increasing the number of varactor cells does not affect the tuning range, however improves the Q by reducing the value of equivalent parasitic resistances. Q of the

varactors however, shows a negligible improvement by increasing the varactor size after a certain point. Thus, a reasonable varactor size should be selected by considering practical values of the base inductance in Figure 6. (see Equation 7.)

2) Based on Equation 2-3 there is an optimum value for the capacitance ratio, n (Equation 5), that minimizes the phase noise of the VCO, independent of the biasing condition and Q. It is worth mentioning that Equation 3 only includes the phase noise contribution of collector current shot noise and tank resistance. In [91], considering the contribution of all noise sources, the optimum value of "n" was found numerically to be approximately 0.3. A same value of n was also found to provide the minimum phase noise in the present design.

3) Having found C_{var} and "n" from steps 1-2, calculate the value of total capacitance and the base inductance LB for the target oscillation frequency using Equation 7. This inductance must be designed to achieve the highest achievable Q by increasing the width of the T-line without exceeding the self-resonance frequency.

4) Find the equivalent Q of the tank and calculate the value of equivalent tank impedance (RT). considering the breakdown voltage of the devices, choose the supply voltage and find the maximum value of Atank that keeps Q1 and Q2 away from entering the saturation region and calculate IC using Equation 2.

5) Find the size of SiGe HBTs which provides peak f_{max} when biased at IC and calculate the value of the base-emitter capacitances C1 and C2 using Equation 6.

6) Design the output matching network for the targeted load using load-pull

simulations.

Clearly the above procedure is an iterative methodology, however, it provides an insight for the design and optimization of the mmW Colpitts VCO with minimum number of iterations.

The cascode configuration provides several advantages in the design of the VCO, although it can introduce some additional noise, which slightly degrades the overall phase noise. First, it isolates the VCO core from the frequency dividers and reduces the frequency-pulling effect. Secondly, it provides higher output power by permitting a larger output swing due to the higher collector-base breakdown voltage. The low impedance at base terminal of the cascode SiGe HBTs allows fast depletion of hot carriers from the transistor active area upon impact ionization. This in fact increases the breakdown voltage of the collector-base junction to BVCBO, which is 4.5 V in this process technology. In addition, cascode devices provide very small impedance to the collector of the Colpitts core, helping ensure robust oscillation [85].

To further increase the output power and power efficiency, load-pull simulations were used to design a wideband matching network at the output of the VCO. The entire layout of the circuit was fully EM-simulated using Sonnet software to precisely predict the electrical performance of the circuit. These simulations included T-lines, MiM capacitors, resistors, as well as transistor interconnections.

2.2.1 Low Phase Noise and High Output Power 367 GHz and 154 GHz Signal Sources

Design of the differential LO distribution network and routing is challenging at high

frequencies and requires additional amplification and buffering. Besides additional DC power consumption and die area, the amplifiers should provide wide bandwidth to cover the entire tuning range of the VCO, as well as provide extra margin in the case of any frequency shift.

In the present design, coupled VCOs were proposed for signal generation and driving the output and frequency dividers. This technique facilitates LO distribution, simplifies the differential layout, and improves the overall phase noise. In addition, by utilizing this approach, the balanced signals of the VCO becomes available for higher output power or differential drive of the power-amplifier (PA) or frequency-doublers.

Figure 7 shows the schematic of the proposed coupled VCO topology. The conceptual block diagram of this circuit is shown in Figure 8. The idea behind this scheme is to couple each branch of the Colpitts VCOs to nearby VCO by direct current injection using the combination of LB, LE and varactors. Since the entire oscillation current is directly injected to the other VCO, a strong coupling is established between the nearby branches of the coupled VCOs. The left and right branches are coupled differentially using base inductors and varactors following the conventional differential Colpitts topology.

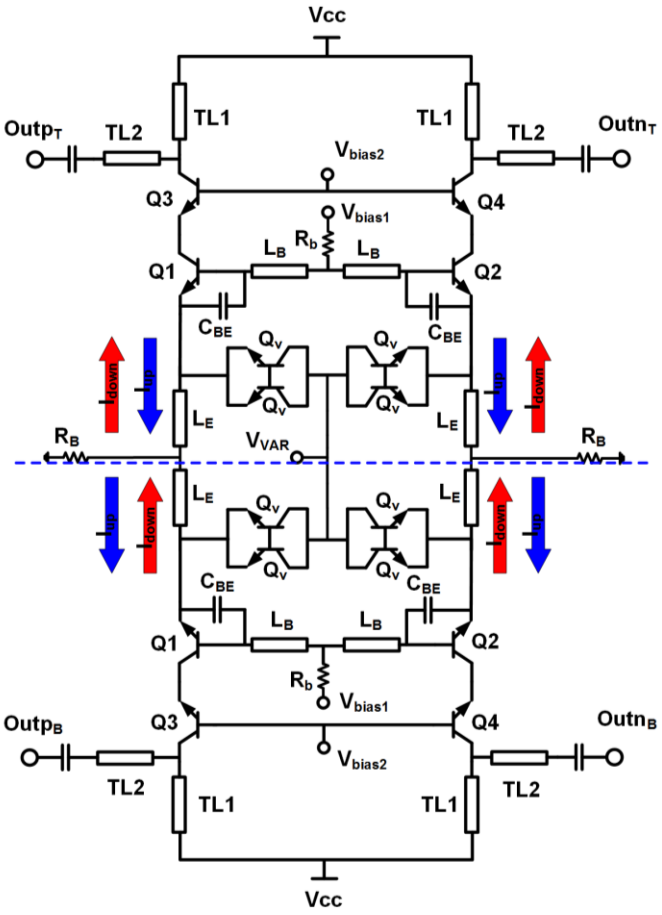

Figure 7. Schematic diagram of two coupled Colpitts VCOs.

Biasing resistors at common base nodes prevent common mode excitation and assure a differential coupling between the left and right branches. The top and bottom VCOs however, can be coupled either in differential mode or in common mode using direct current injection by LE inductors and depending on the design of LE inductors. In the present design, the top and bottom VCOs are coupled in common mode. Therefore, the top and bottom VCOs are oscillating in phase, while the left and right VCOs are oscillating out of phase.

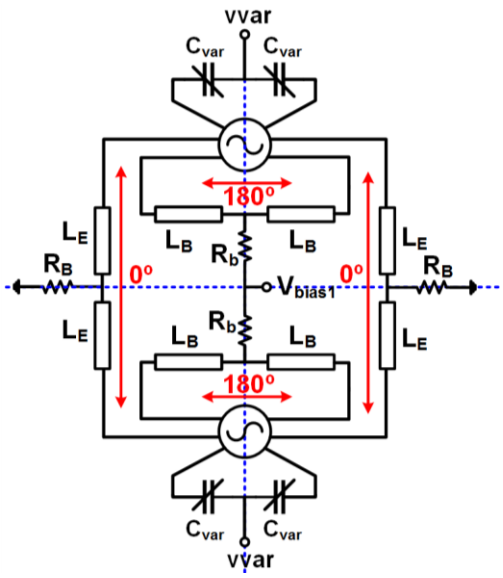

Figure 8. Block diagram of the coupled LC Colpitts VCOs.

A modified version of the current technique was originally presented in [14] for phase locking 4-free running radiating push-push VCOs in differential mode at 316 GHz.

Figure 9 shows the simplified ac model of the standalone VCO for common mode and differential mode coupling between top and bottom VCOs. It can be shown that oscillation frequency of the coupled VCOs in differential mode, can be calculated by solving the equality in Equation 8. This is the same frequency in which the impedance of the series resonator tank, looking from the base of the VCO becomes zero. The equivalent negative resistance can be calculated using Equation 9 and Equation 10. The negative resistance in differential mode is proportional to equivalent impedance of the varactor capacitance and LE inductance. Thus, by controlling LE, the magnitude of the equivalent negative resistance in differential mode can be controlled without affecting the common mode operation.

$$L_B s + \frac{1}{C_{BE} s} + \frac{1}{C_{var} + \frac{1}{L_E s}} = 0 \qquad (8)$$

$$R_{NEG-diff} = \frac{g_m}{C_{BE} s \left(C_{var} s + \frac{1}{L_E s} \right)} \qquad (9)$$

$$R_{NEG-comm} = \frac{g_m}{C_{BE} s (C_{var} s)} \qquad (10)$$

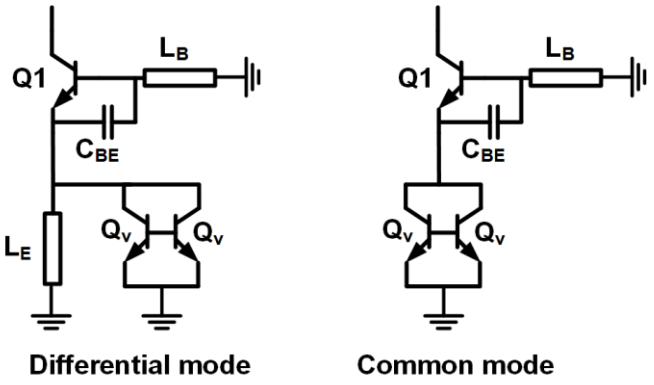

Figure 9. Simplified ac model of the standalone VCO in common mode and differential mode coupling of top and bottom VCOs.

Figure 10 shows the simulated negative resistance of the coupled VCOs by varying the inductor LE. The negative resistance was observed from the base of Q1 SiGe HBT (see Figure 7). The magnitude of the negative resistance of the common mode is larger than differential mode independent of the value of LE, thus the common mode is the dominant oscillation mode in this architecture. However, it is important to completely prevent the excitation of the differential mode to assure that entire network operates in a single mode under any circumstance. By decreasing the value of LE, one can decrease the magnitude of negative resistance of differential mode in such a way that it becomes smaller than the resonator loss, thus, the excitation of the differential mode can effectively be prohibited while the common mode operation remains unchanged due to insensitivity to the value of LE in common mode operation. Figure 11 shows the simplified 3D layout of the coupled

VCOs. Differential power generation and division can be performed at the same time and in a compact form factor with excellent symmetry. One VCO feeds the frequency dividers, while the other provides differential signals to the output of PLL.

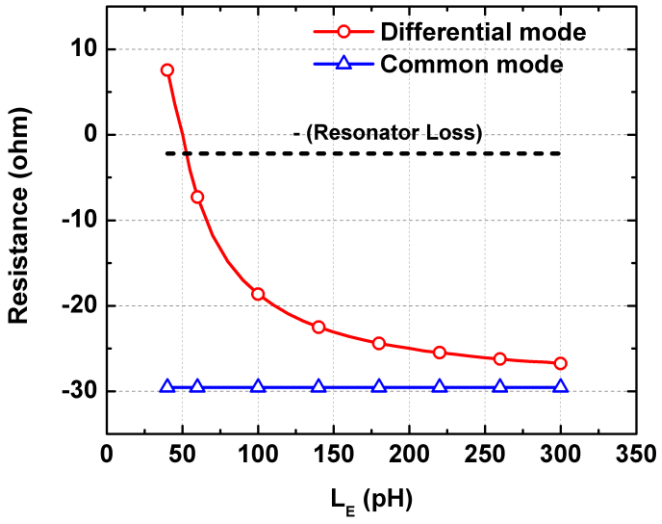

Figure 10. Simulated small signal negative resistance of the coupled VCOs looking from the base of Q1 SiGe HBT for both differential and common mode operation.

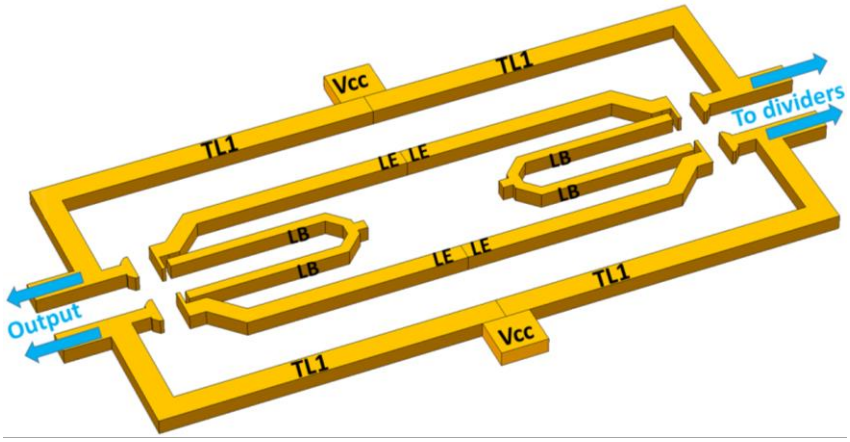

Figure 11 3D view of the simplified layout of the coupled VCOs. One VCO feeds the frequency dividers with differential signals, and the other VCO drives the output load.

The complexity of differential routing to the output and the dividers are significantly reduced. Moreover, both the output and frequency dividers can receive the entire balanced RF power of VCOs to boost the output power and enhance the locking

range of frequency dividers. In addition, the present coupling methodology does not change the performance parameters of the standalone VCOs. Therefore, the design procedure of the coupled VCOs can be reduced to the design of the standalone VCO.

It is known that coupling the signal sources improves the phase noise of the coupled network. Detailed analysis of the phase noise of coupled oscillators can be found in [93]. It is straight forward, however, to understand the phase noise improvement by considering the phase noise analysis presented in [88], [94], [95]. Equation 11-12 defines the phase noise of generic oscillator using ISF [88].

$$\boldsymbol{L(\Delta\omega) = 10.\log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}.\frac{\bar{\imath}_n^2}{4.\Delta\omega^2}\right)} \qquad (11)$$

$$\boldsymbol{\Gamma_i(x) = \frac{f_i'}{\left|\overrightarrow{f'}\right|^2} = \frac{f_i'}{\sum_{j=1}^{j=n} f_j'^2}} \qquad (12)$$

$\Gamma_i(x)$ is the ISF when the impulse is applied to ith node, q_{max} is the maximum charge displacement in the resonator, $\bar{\imath}_n^2$ is the injected noise at ith node, $\left|\overrightarrow{f'}\right|^2$ is the norm of the first derivative of the waveform vector, and f_i' is the derivative of the normalized waveform on node i. Here, the state variables are node voltages (see [88] for more details). In the case of N coupled VCOs, there are N equal state variables for each state variable present in a single VCO, thus considering Equation 12, the ISF of the coupled network is reduced by the factor of N (Equation 13.).

$$\boldsymbol{\Gamma_{i,Ncoupled}(x) = \frac{f_i'}{N.\sum_{j=1}^{j=n} f_j'^2} = \frac{\Gamma_i(x)}{N}} \qquad (13)$$

Based on Equation 11, the contribution of each noise source on the overall phase noise of the coupled VCOs is reduced by the factor of N^2, however, since the number of

noise sources in the coupled network is N times the number of noise sources present in a single VCO, the overall phase noise of the coupled VCOs is only improved by the factor of N (Equation 14).

$$\boldsymbol{L_{N,coupled}(\Delta\omega)} = \mathbf{10.log}\left(\boldsymbol{N}.\frac{\boldsymbol{\Gamma_{rms}^2}.\boldsymbol{1/N^2}}{\boldsymbol{q_{max}^2}}.\frac{\boldsymbol{\bar{\imath}_n^2}}{\boldsymbol{4}.\boldsymbol{\Delta\omega^2}}\right) = \mathbf{10.log}\left(\frac{\boldsymbol{\Gamma_{rms}^2}}{\boldsymbol{N}.\boldsymbol{q_{max}^2}}.\frac{\boldsymbol{\bar{\imath}_n^2}}{\boldsymbol{4}.\boldsymbol{\Delta\omega^2}}\right) \quad (14)$$

Figure 12 compares the simulated normalized Γ functions of the proposed coupled VCOs with the standalone VCO. A theoretical 2X reduction of the Γ of the coupled VCOs can be observed from this figure. Circuit-level simulations were performed in ADS to investigate the achievable phase noise improvement. Figure 13 shows the comparison of the simulated phase noise between the standalone VCO and the coupled VCOs. An improvement of 3 dB can be observed from this simulation, which matches the expected theoretical value. Since the proposed PLL locks the phase of one of the VCOs to the reference clock, any mismatch of the components within the coupled VCOs can potentially lead to a static phase error with the reference clock at the output of the PLL which can be a concern for certain applications. Figure 14 shows the simulated static phase error between the balanced outputs of the coupled VCOs, due to mismatch in components. Exaggerated mismatch values were used in this simulation, however, the real component mismatch in the current fabrication technologies is much smaller. Simulations show that small static phase error is created even with the presence of large mismatch values.

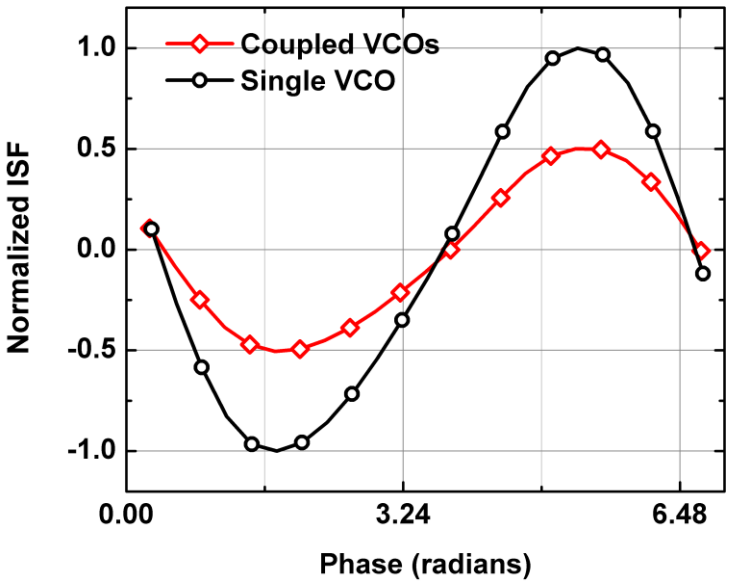

Figure 12. Simulation results of the normalized Γ functions of the standalone VCO, compared to the coupled VCOs. The Γ functions were normalized to peak value of the Γ of the standalone VCO for easier comparison.

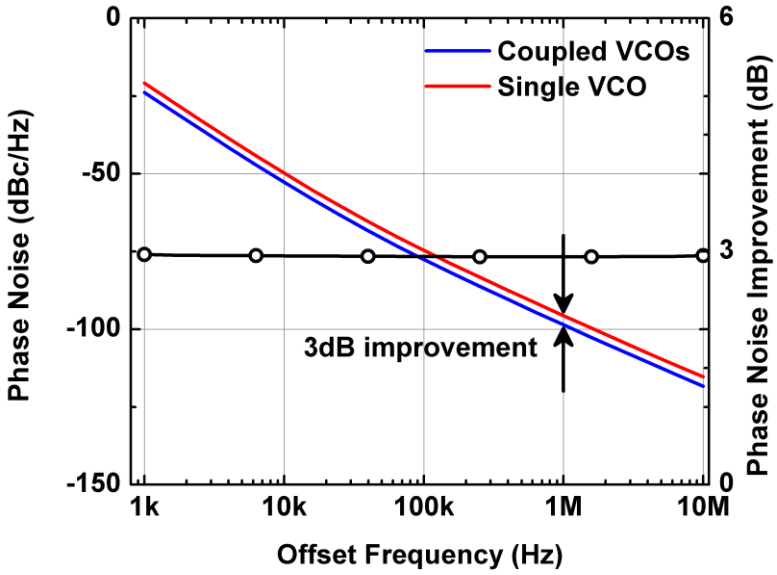

Figure 13. Simulation results of the comparison between the phase noise of the standalone VCO with phase noise of two coupled VCOs.

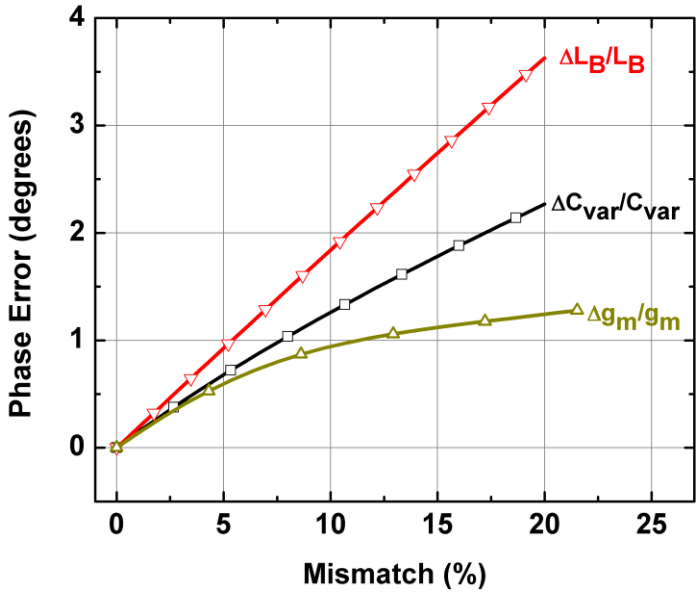

Figure 14. Simulated static phase error between the balanced outputs of coupled VCOs because of component mismatch.

2.3 PLL Design

Figure 15 shows the block diagram of the designed integer-N D-band PLL. Frequency multiplied crystal oscillators with oscillation frequencies at multiples of 100 MHz exist in small form-factor for the input reference clock. Nevertheless, relatively low power and simple on-chip frequency multipliers can be designed to multiply the input reference frequency if needed. The selected reference frequency for this PLL was 450 MHz. Therefore, a large division factor was needed for frequency division from D-band frequencies. Due to the large division factor, the phase noise of the individual components experiences large amplification factors when transferred to the output of the PLL. Combined with high KVCO value of the high frequency VCO, the contribution of some of the noise sources that are insignificant at lower frequency PLLs may become considerable in this mmW design. Thus, a careful loop design and optimization was required.

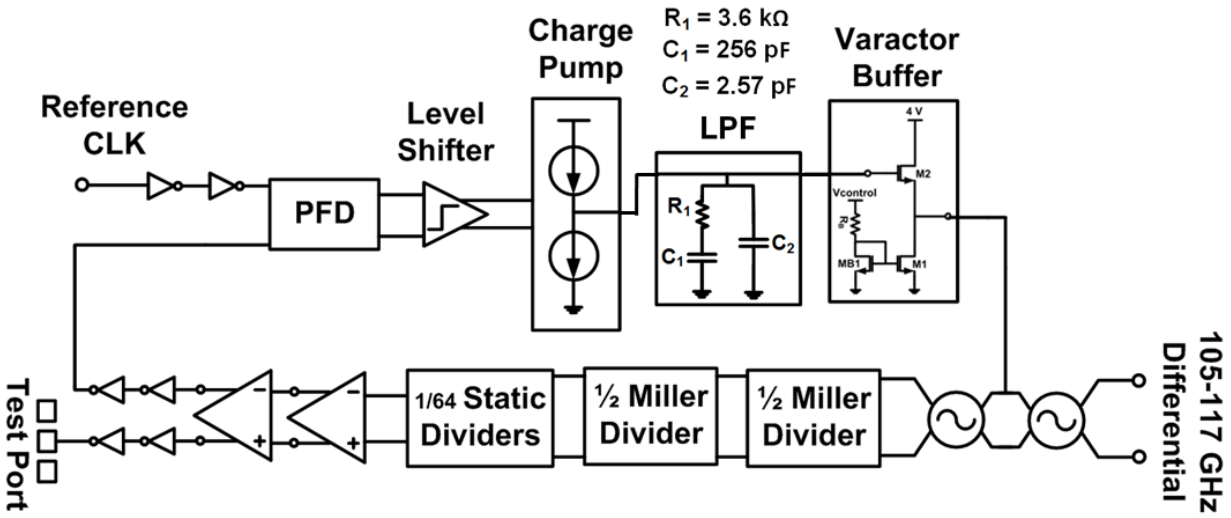

Figure 15. Block diagram of the D-band integer-N PLL.

To simulate these effects and design the loop dynamics accurately, a linear model in the phase-domain was created in MATLAB. A commonly used second-order low-pass filter was utilized as the loop filter (see Figure 15.). Because of the relatively high reference frequency, the problem of the spur was considered secondary concern in the present design, thus, a smaller damping capacitor can be utilized. Therefore, the second pole of the loop filter can be placed at higher frequencies. A relatively low frequency zero can then assure adequate phase margin for a stable loop across the various charge pump currents and KVCO. The frequency of the zero and second pole were 173 kHz, and 17.3 MHz in this design, respectively (Equation 15-16). A stable loop operation with a phase-margin of greater than 65° across various charge pump currents can be obtained with this choice. By increasing the charge pump current, the DC gain of open-loop transfer function increases and as a result, the crossing frequency also increases however, since the frequency of the second pole is far enough from the frequency of the zero, it can only negligibly degrade the phase margin of the system. Thus, the PLL bandwidth can be controlled by varying the charge pump current without any stability concerns. Figure 16 shows the simulated phase

margin and bandwidth of the loop for various charge-pump current selections.

$$\omega_z = \frac{-1}{R_1 C_1} = -1.085\ MRad/\sec \quad (15)$$

$$\omega_{p2} = \frac{-1}{R_1 \cdot \frac{C_1 C_2}{C_1 + C_2}} = -109\ MRad/sec \quad (16)$$

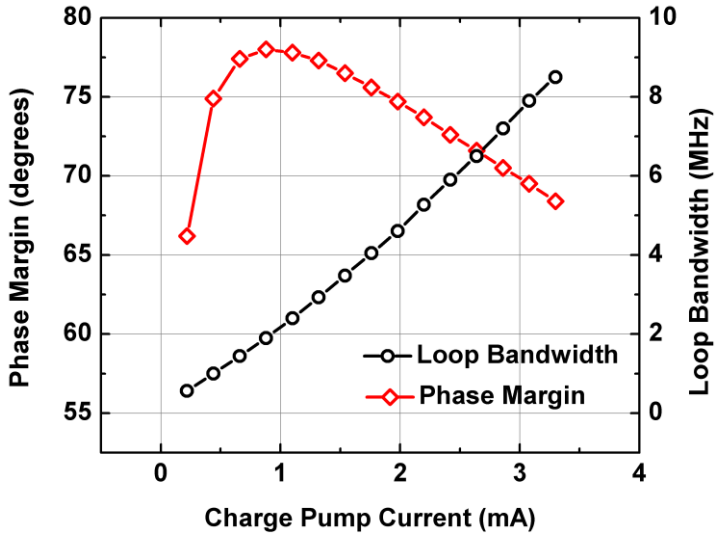

Figure 16. Simulated results, showing the control of loop bandwidth by controlling the charge pump current.

2.3.1 Frequency Divider

Wideband operation is one of the key requirements for this design. Since the VCO tuning range is the main limiting factor of the locking-range, the frequency dividers should be wideband enough to sufficiently overlap the VCO tuning-range in case of any unexpected frequency shift. Injection-locked frequency dividers are a popular choice for the design of mmW dividers; however, the narrow locking-range of these types of dividers makes them less attractive for the present design. Miller-based regenerative frequency dividers, on the other hand, can operate in a broad bandwidth well above the frequencies that static dividers can operate. Miller dividers were chosen as the first two frequency

divider blocks for the present design. The rest of the dividers are static dividers that can operate over wide frequency ranges.

Dynamic Miller dividers were originally proposed by Miller in 1939 [96]. The output of this divider is mixed with its input in a feedback loop to regenerate a signal at half of the input frequency. A detailed explanation of the operational principal of the circuit can be found in [97]. A popular implementation of this circuit utilizes a differential Gilbert cell as the mixer core, where the output of the mixer is fed back to its input to create a regenerative loop. Two possible implementation schemes of this circuit are shown in Figure 17. Emitter-follower buffers provide a necessary phase shift for proper operation of the regenerative loop. This configuration can possibly sustain two output frequencies at $\frac{\omega_{in}}{2}$ and $3\frac{\omega_{in}}{2}$.The parasitic capacitors of the SiGe HBTs combined with the inductive short stubs, form a resonant tank which effectively suppress the 3rd harmonic of the divided signal.

An important design consideration here, is the possibility of instability of the Miller divider when utilized in scheme (b) in Figure 17. The presence of the input transmission lines, combined with the parasitic capacitances of the transistors shown in Figure 17. (b), can potentially cause a positive feedback. This positive feedback can cause unwanted oscillation. Care must be taken when using this topology to avoid instability problem. For this reason, scheme (a) was selected for the implementation of the first two frequency dividers. The circuit was carefully laid out in a symmetric form and EM simulations were

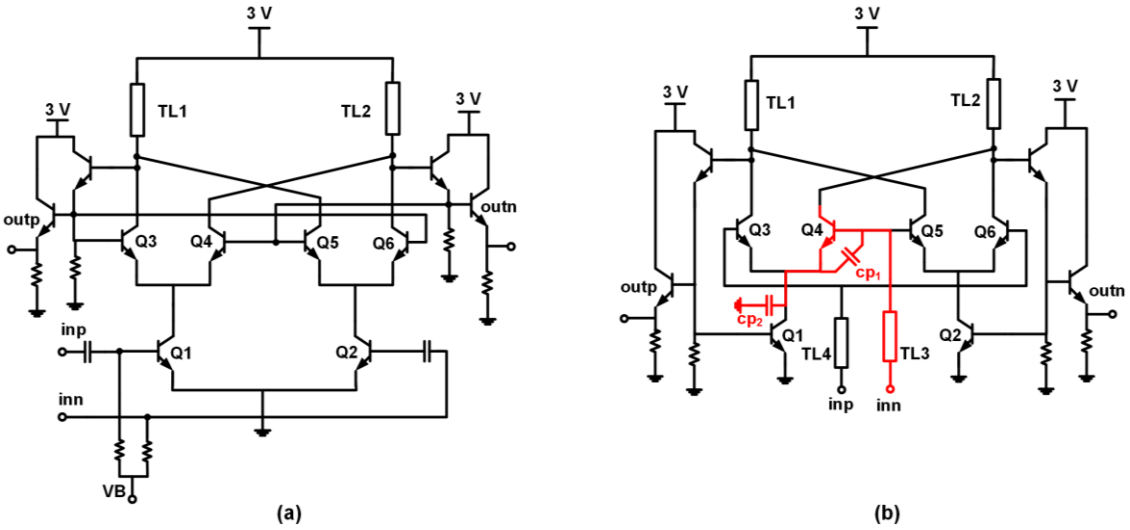

Figure 17. Two configurations for the realization of the dynamic Miller divider. feedback from the output of the divider to the input of switch transistors (a). feedback from the output of the divider to input of the gm transistors. (b).

performed to model the effect of interconnections and transmission lines. The transistor interconnections (vias) were still short enough in this frequency so that parasitic RC extraction could fully capture the layout parasitics. The center frequency of the dividers was designed to match the VCO. This allows maximum possible margin for any frequency deviation due to process variations. Figure 18 shows the simulated input sensitivity curve of the designed Miller dividers. Locking range of these dividers depends on the applied input power. The high output power of the coupled VCO topology insures a wide locking range for the frequency dividers. Simulation results show that the first Miller divider can divide across a wide frequency of 75-153 GHz, while the second Miller divider can successfully divide across a frequency range of 35-75 GHz.

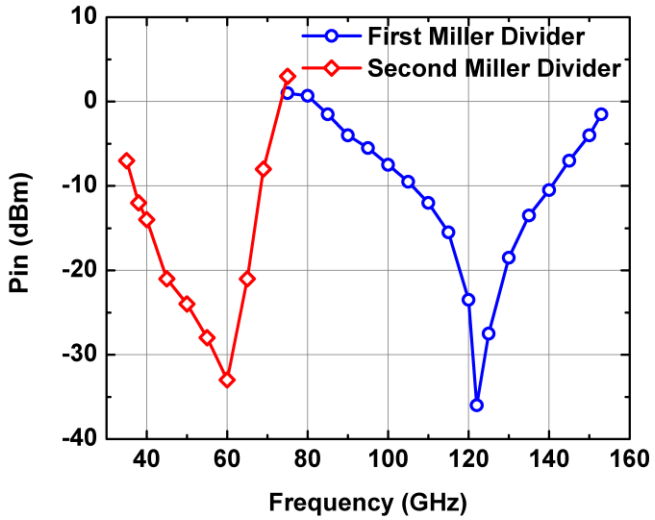

Figure 18. Simulated input sensitivity curve of the first two regenerative frequency dividers.

2.3.2 Charge Pump and Loop Filter

To further increase the tuning range of the VCO, a supply voltage of 4 V was chosen for the charge pump circuit. Since the output of the digital circuits and phase-frequency detector (PFD) is 2 V, extra level-shifting gates were designed to convert the digital level of 2 V into a digital level of 4 V. Figure 19 shows the schematic of the charge pump circuit. Because of the large clock swing, this topology was chosen, which effectively eliminates the clock feedthrough to the output. The biasing voltage of the charge pump can be increased further to enhance the tuning range of the VCOs. High-breakdown MOS devices were utilized in the design of charge pump in order to handle the large supply voltage of charge pump utilized. The M3 and M4 MOSFETs are the main current pumping transistors that are controlled with the QA and QB digital inputs. The MBi transistors are used for biasing and mirroring the biasing current to up and down push-pull branches. Details of this topology can be found in [98]. Inclusion of the pass-gate equalizes the delays in charge pump input branches to reduce reference spurs. The gate length of the high-breakdown

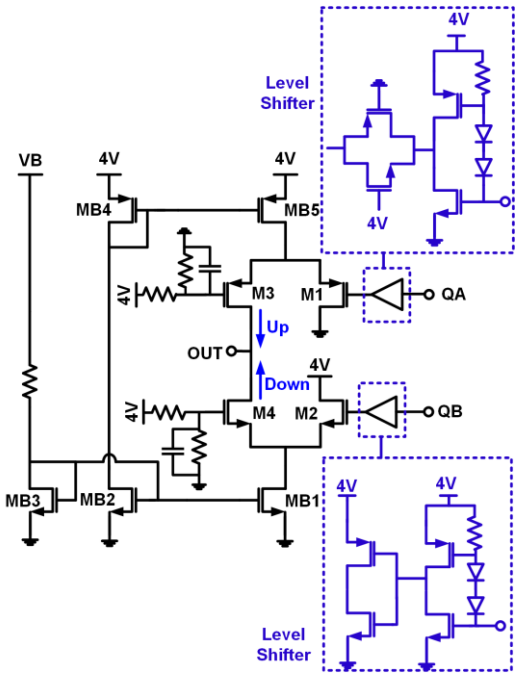

Figure 19. Circuit schematic of the charge pump circuit.

MOSFETs was 0.35 µm, Thus, these devices experience less short channel effects. An interesting phenomenon was observed while simulating the PLL together with the charge pump. The PLL failed to lock at the lower frequency ranges of the VCO, even while all the components were operating under normal operational conditions. After a full investigation of the functionality of the system and its building blocks, It was found that due to the large swing of the VCO signal, the varactors partially enter the saturation region at the peaks of the signal swing and conduct some DC current particularly at lower frequencies (smaller control voltage), and thus the current of charge pump circuit was partially sunk into the varactors, resulting in the PLL failing to lock. To remedy this problem, a source- follower buffer was designed after the loop filter to drive the varactors. This buffer does not change the dynamics of the loop, assuming it has enough linearity; however, it isolates the charge pump from the varactors and compensates for the leakage current of the varactors. This prevents any change in the current of the charge pump circuit

and prevents any potential locking failure. The only drawback of this approach is the additional noise that is introduced into the PLL loop, which can possibly degrade the phase noise of the circuit. Simulation results show that adding the buffer introduces some additional flicker noise and degrades the phase noise at the lower offset frequencies of the signal, while negligibly affecting the noise behavior of higher offset frequencies. Large CMOS transistors can be utilized for this buffer at this slow node to minimize the flicker noise contribution to the overall phase noise. Figure 20 shows the schematic of the source-follower buffer, as well as simulation results showing the contribution of the buffer on the phase noise of the VCO.

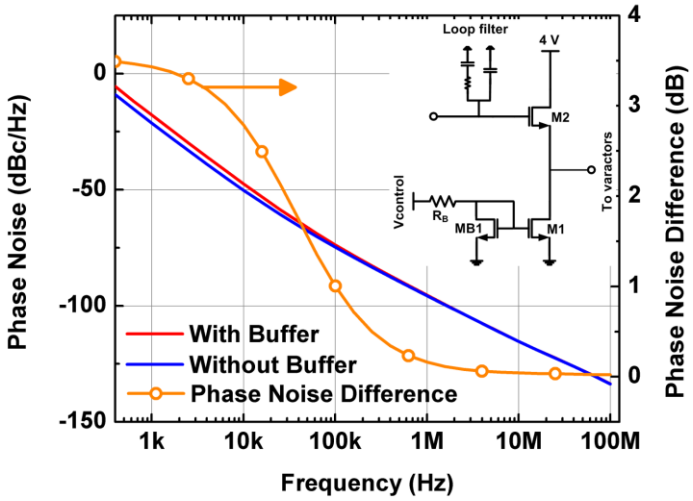

Figure 20. Schematic of the varactor buffer, and simulation results showing the effect of this buffer on the phase noise performance of the VCO.

The phase noise at lower offset frequencies was degraded because of the flicker noise from the buffer; however, the phase noise at higher offset frequencies was affected negligibly. The transfer function from the buffer noise to the output of PLL has high-pass characteristics, similar to the transfer function of the VCO noise components. Thus, the flicker noise from the buffer can effectively be filtered out by the PLL loop. Figure 21

shows the simulation results of the PLL phase noise with and without including the buffer inside the loop. The additional noise from the buffer was completely filtered out with the PLL loop and the total phase noise of the PLL remained unchanged. Measurement results shows no change on the phase noise behavior of the PLL by changing the biasing current of the buffer and verifies this fact.

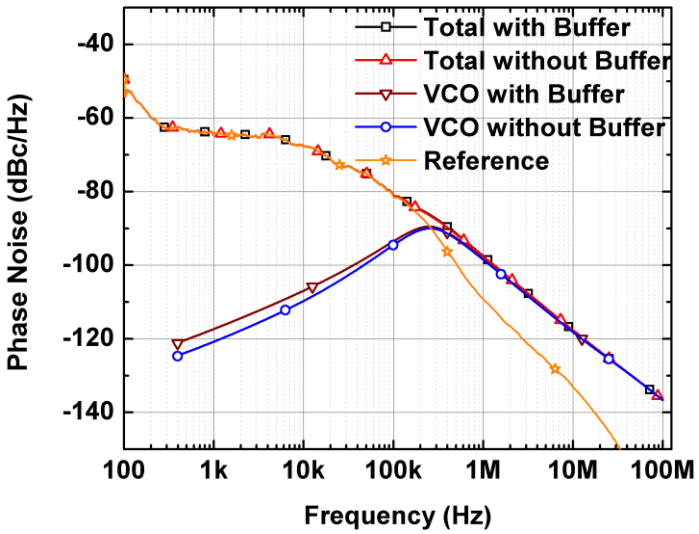

Figure 21. Simulated PLL phase noise using the linear-phase model. Measured phase noise of the reference clock was utilized in this simulation. The total phase noise of the PLL with varactor buffer remains unchanged.

In addition, the phase noise at lower offset frequencies tracks the phase noise of the reference signal with no indication of any additional noise contribution, demonstrating that inclusion of the buffer within the loop does not affect the phase noise performance of the PLL. This technique extends the locking range of the PLL and prevents the change of charge pump current.

2.3.3 Buffers

To provide full-range rail-to-rail and clean digital signals, amplifiers and buffer

circuits were designed following the last frequency divider and at the input of the reference clock. (see Figure 15.). Figure 22 shows the schematic of these buffers. Resistive feedback differential amplifiers enhance the output swing of the last frequency divider, such that it could completely switch the subsequent inverter buffers. Inclusion of the resistive feedback with large resistor values precludes the requirement of common-mode feedback for the differential amplifiers.

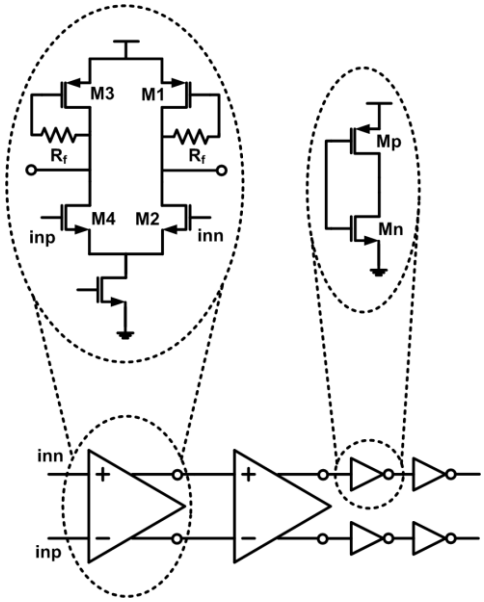

Figure 22. Schematic diagram of the buffer circuits in the PLL loop.

2.4 Measurement Results

A standalone VCO test structure was first measured. The oscillation frequency of the standalone VCO was slightly shifted from that of the coupled VCOs inside the PLL, due to difference in emitter transmission line interconnections of the VCO test structure. The measured spectrum of the VCO after down-conversion with an OML T/R module and amplification at IF port is shown in Figure 23. By slightly shifting the LO frequency, the down-converted signal with the 10^{th} harmonic of the LO signal was identified. The output

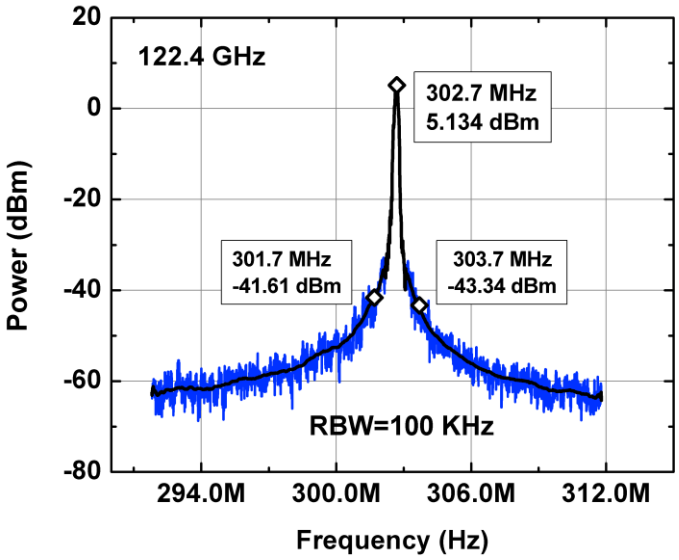

Figure 23. Measured spectrum of the standalone free running VCO after down-conversion with 10X OML T/R downconverter and amplification at IF port.

power of the VCO was measured using an Erickson PM2 calorimeter. The losses from the probe and waveguide connections was first measured and de-embedded using the PNA with OML extender modules. Figure 24 shows the measured output power of the VCO. The VCO can generate more than +10 dBm of average power across the entire tuning range and under nominal biasing conditions. Higher output power can be quite useful in larger systems where the LO must be distributed across several blocks within the system. The output power of this VCO can be further increased by aggressively biasing the transistors beyond the safe operating area. It has been shown that SiGe HBTs can reliably operate above the DC breakdown limits when high power RF signal is applied [99]. Figure 24 also includes the measurement results of the output power of the VCO under aggressive biasing conditions. The output power of this VCO was safely increased to more than +14 dBm.

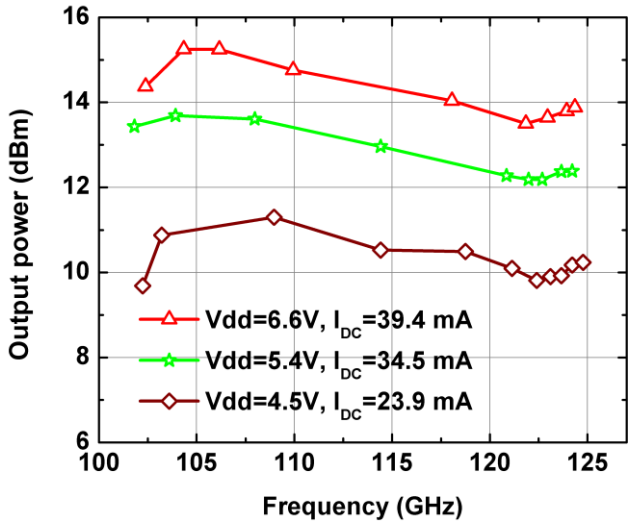

Figure 24. Measured output power of the VCO across the tuning range. One of the output branches of the differential circuit was terminated on-chip, thus a single-ended measurement was performed and 3dB value was added to the measured data.

For a VCO operating as an autonomous circuit, and without the applied input power, the power-added-efficiency (PAE) and power-efficiency (PE) metrics are equal. The efficiency of VCOs are typically much smaller than the efficiency of PAs. However, with a careful design in analogy with the design of PAs, higher efficiencies can be obtained. The Colpitts topology inherently operates in class-C and the transistors turn ON in only a fraction of the signal period, and thus an improved PE can be achieved by designing for maximum output power. Load pull simulations were utilized to design the output matching network for maximum power transfer. Figure 25 shows the measured PE of the VCO across the tuning range and under various biasing conditions. The present design achieves an average power efficiency of 10%. Table 1 compares the performance of this VCO with reported state-of- the-art designs. The designed VCO achieves the highest FoM_T at D-band frequencies.

Table 1 Performance summary of the VCO compared to state-of-the-art.

Ref	Frequency (GHz)	Tuning range (%)	Phase noise @ 1MHz (dBc/Hz)	Phase noise @ 10 MHz (dBc/Hz)	Output power (dBm)	Power efficiency (%)	P_{DC} (mW)	Tech	FOM_T	FOM
[28]	92.5-100.5	8.3	-102	-124.5	+6	4.4	90	130nm SiGe	188.7	190.3
[29]	104-108	4	-101.3	-	+2.5	1.34	133	130nm SiGe	174.9	182.9
[46]	69-92	29	-97	-	+12	6.5	244	0.35µ SiGe	192.6	183.3
[47]	147-159	7.8	-96	-119	+9	6	132	130nm SiGe	185	182.8
This work	102.4-124.4	19.4	-96.9	-117.4	+10.5	10	110	130nm SiGe	194.38	188.6

$$FoM_T = 10\,log10\left[\left(\frac{f_0}{\Delta f}\right)^2 \cdot \frac{1}{L(\Delta f)} \cdot \frac{P_{out}}{P_{DC}} \cdot \left(\frac{TR(\%)}{10}\right)^2\right]$$

$$FOM = 10\,log10\left[\left(\frac{f_0}{\Delta f}\right)^2 \cdot \frac{1}{L(\Delta f)} \cdot \frac{P_{out}}{P_{DC}}\right]$$

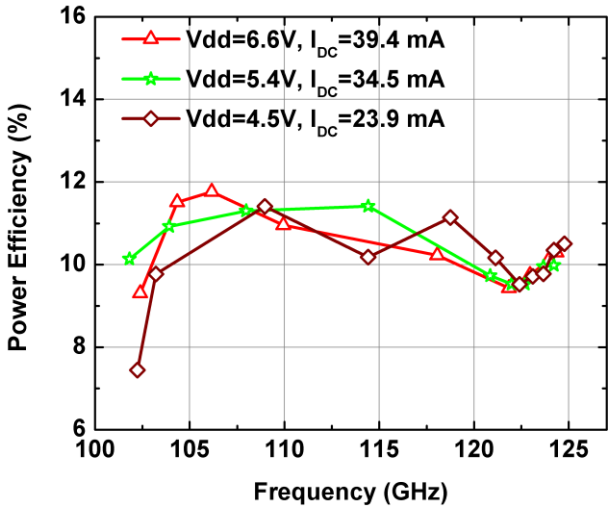

Figure 25. Measured power efficiency of the standalone VCO at various biasing conditions.

Figure 26 shows the die micrograph of the PLL. The circuit was fully-integrated in IHP's 130 nm SiGe BiCMOS technology. The chip measures 1.5×1.4 mm^2 including the pads. The DC consumption of the circuit is 0.6 W when operating in nominal biasing conditions. The DC consumption can be reduced by utilizing CML frequency dividers at lower frequencies. This PLL locks from 105 GHz to 117 GHz under nominal biasing

conditions, with 10.8% of locking range. The PLL was measured using a D-band T/R extender module from OML. This module was utilized as a down-conversion mixer for this measurement. The module operates as a 10th harmonic down-conversion mixer.

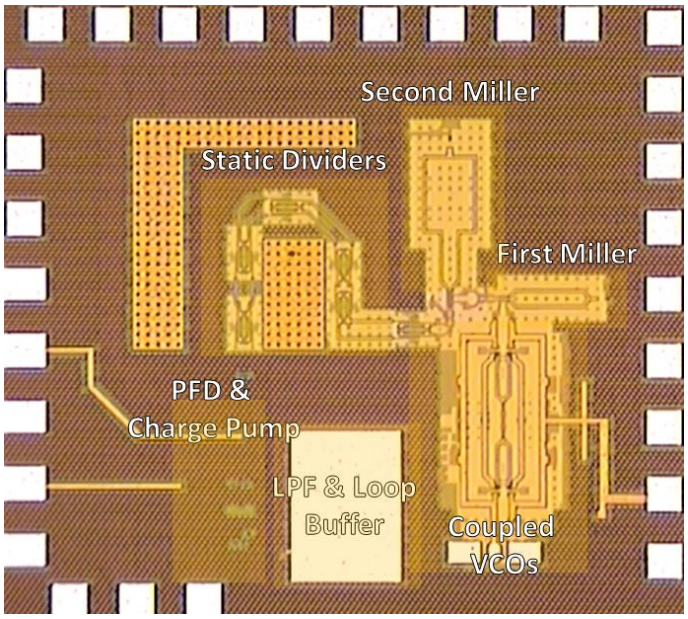

Figure 26. Die photo of the fully integrated D-band PLL.

An external LO signal was fed into the T/R extender and the IF signal was collected from the module. Figure 27 shows the measurement setup. An HP 83712A signal generator was used as the low frequency reference signal to the PLL. Therefore, the close-in phase noise of the circuit was limited to phase noise of this instrument. An Agilent EE4446A spectrum analyzer with built-in phase noise personality software was used for measuring the spectrum and phase noise of the signals. Figure 28 shows the measured phase noise of the PLL at an output frequency of 115.4 GHz.

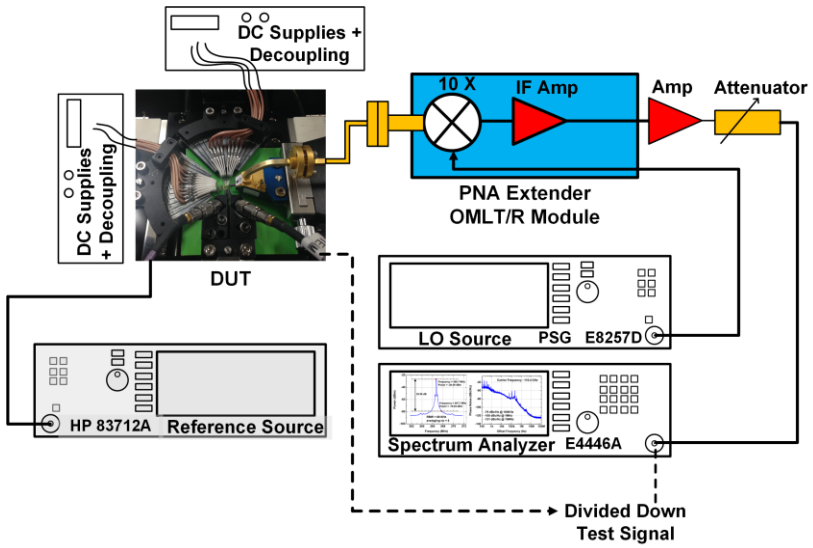

Figure 27. Measurement setup for measuring the phase noise and signal spectrum.

The generated signal achieves a low phase noise performance of -100 dBc/ Hz and -121 dBc/ Hz at 1 MHz and 10 MHz offset from the carrier, respectively. The observed spurs in low frequency offset frequencies arise from the reference signal generator. The close-in phase noise of the output signal is dominated by reference phase noise, while the phase noise at higher offset frequencies is mostly dominated by the phase noise performance of the VCO. The slope of 20 dB/dec continues beyond the 10 MHz offset from the carrier, and follows the phase noise performance of the standalone VCO without being affected by additional noise from the loop filter, achieving a record value of -121 dBc/Hz at 10 MHz offset from the carrier. These results agree well with our system-level simulation results presented in the previous sections.

Figure 29 shows the measured spectrum of the signal after down-conversion with the OML extender module. The clean and sharp spectrum is the indicative of excellent phase noise performance of the PLL.

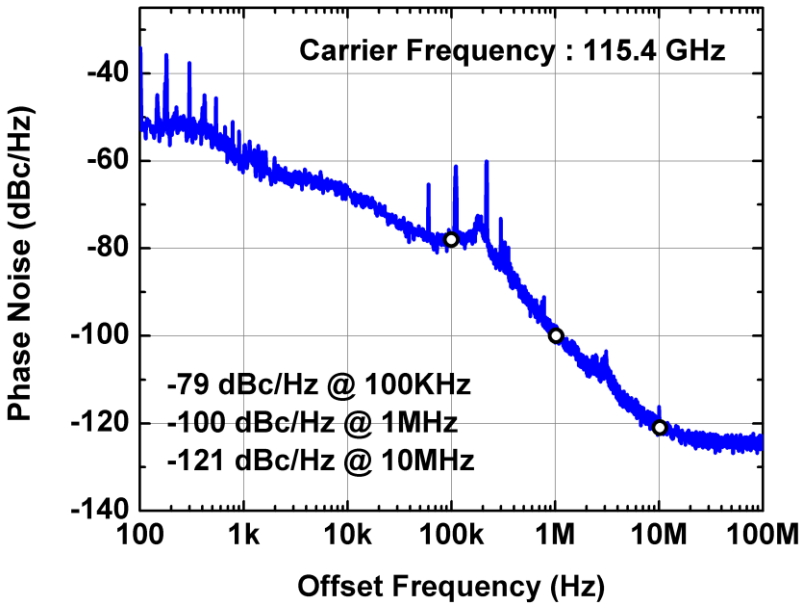

Figure 28. Measured phase noise response of the PLL after down-conversion with the 10X harmonic OML T/R module.

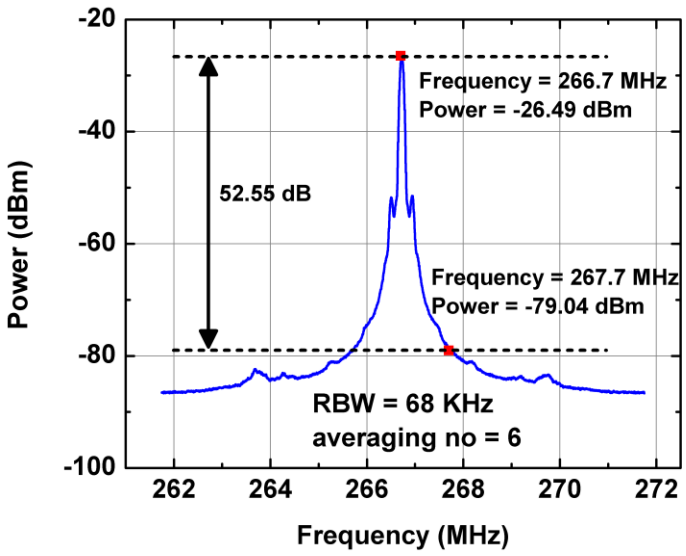

Figure 29. Frequency spectrum of the output signal of the PLL after down-conversion with 10X harmonic OML T/R module.

Figure 30 compares the measured phase noise of the PLL with the phase noise of the same signal after division by 256 at the test port, at the output of the frequency dividers. A theoretical difference of $20log_{10}(256)$ can be observed between the phase noise of these

signals at lower offset frequencies. The discrepancy at higher offset frequencies comes from the limited dynamic range of the measurement equipment to measure the very low phase noise of the frequency divided signal. A small discrepancy from the theoretical value of the 48 dB can also be observed at offset frequencies below 1 kHz. The increased phase noise in this region is the result of LO mixing effect after the down-conversion of the high frequency signal using OML module, and will be discussed later in this section.

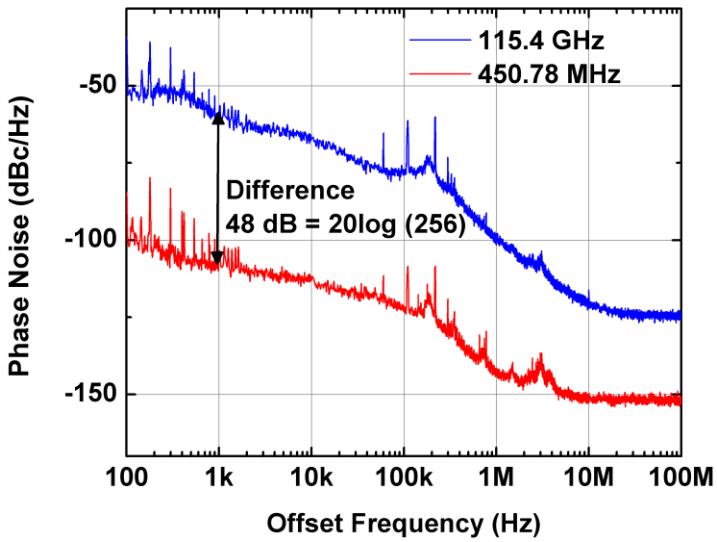

Figure 30. Comparison between the measured phase noise of the PLL output signal at 115.4 GHz with the phase noise of the same signal after frequency division at the output of the frequency dividers.

Figure 31 shows the measured phase noise compared to the simulated overall phase noise of the PLL. Measured phase noise of the reference clock as well as the measured phase noise of the free-running VCO was utilized in this simulation. The measured phase noise of the VCO was reduced by 3 dB in the simulation to account for the phase noise improvement of the coupled VCOs. A good agreement between these data can be observed. It can also be seen that the phase noise of the PLL at offset frequencies below 1 kHz is

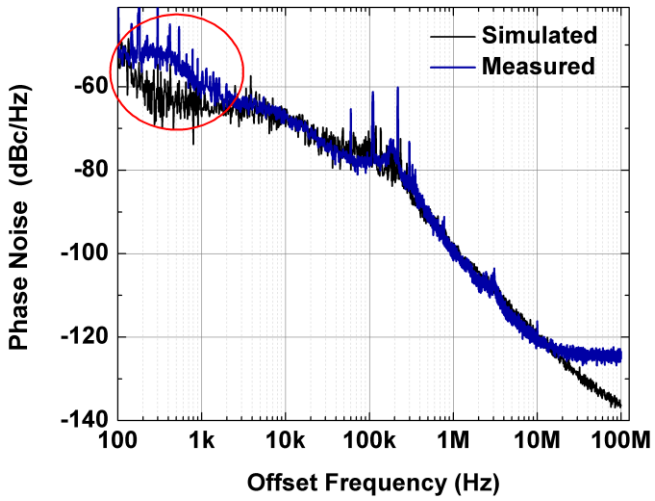

Figure 31. Comparison between the measured and simulated phase noise of the PLL.

higher than the phase noise of the reference signal. Figure 30 shows that this additional noise is not present at lower offset frequencies of the frequency-divided signal. This indicates that this extra noise may come from the down-conversion process. Measurement of the phase noise response of the LO signal reveals that this additional phase noise is coming from the applied LO source which was used to down-convert the output signal. To better understand the relationships between these noise sources, Figure 32 shows the phase noise of the PLL again, together with the phase noise contribution of VCO and other components utilized in simulation setup of the PLL. The phase noise of the LO signal was transferred to output frequency by adding the factor of $20\log_{10}(10)$ to the measured phase noise of the LO signal to account for the 10^{th} harmonic of the LO signal.

Figure 32 shows that the measured phase noise of the PLL perfectly lines up with the transferred phase noise spectrum of different noise contributors at various offset frequencies. One can see that the higher frequency phase noise spectrum of the PLL follows the phase noise response of the standalone VCO, while the low frequency spectrum of the

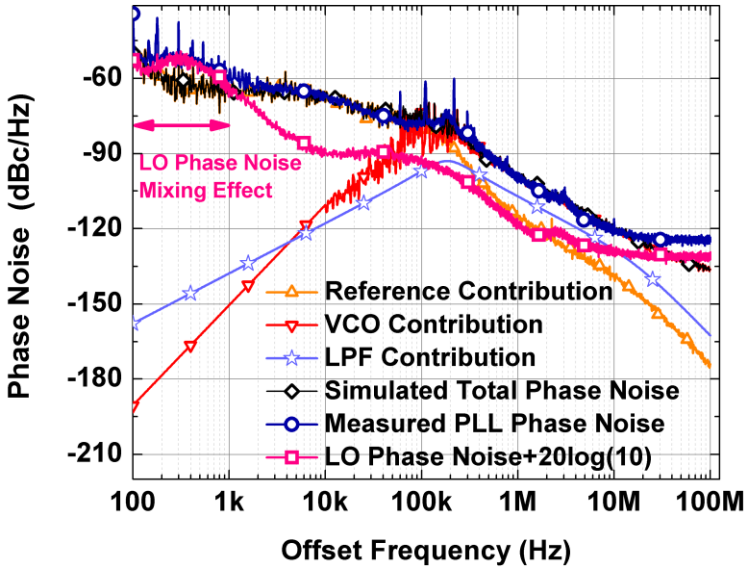

Figure 32. LO mixing effect and the impact of other noise sources in the overall phase noise of the PLL. Phase noise of the reference signal and LO signal was transferred to output frequency by adding the theoretical frequency multiplication factor.

-phase noise follows the phase noise properties of the reference signal. This behavior was expected, due to the frequency selectivity of the PLL loop, with respect to the VCO and reference phase noise, as discussed in the previous sections. The contribution of the LO signal in the overall phase noise of the PLL at offset frequencies below 1 kHz is also clear from this figure and explains the additional phase noise at offset frequencies below 1 kHz. In addition, this plot shows that besides the additional phase noise from the LO source at offset frequencies below 1 kHz, the down-conversion OML module has no impact on the overall phase noise of the PLL.

As mentioned above, the lower offset frequency portion of the PLL phase noise was limited by the purity of the reference clock. Since the reference frequency of this design is relatively low, frequency-multiplied crystal oscillators with low phase noise can be utilized to obtain better phase noise performance. Due to lower phase noise performance

of these types of reference sources, a higher loop bandwidth can potentially result in better phase noise performance by taking advantage of the better transferred crystal phase noise. Figure 33 shows the simulated phase noise of the PLL using the measured phase noise data of pure multiplied frequency crystal oscillator (GMXO-FR), and measured phase noise data of the VCO. The lower offset frequency phase noise of the PLL can be improved using this type of clean reference source. Moreover, one can see that the transferred phase noise of this reference signal is cleaner than the phase noise of the VCO, even at higher -offset frequencies. Therefore, better phase noise performance can be achieved using higher loop bandwidth to further take advantage of the clean reference signal.

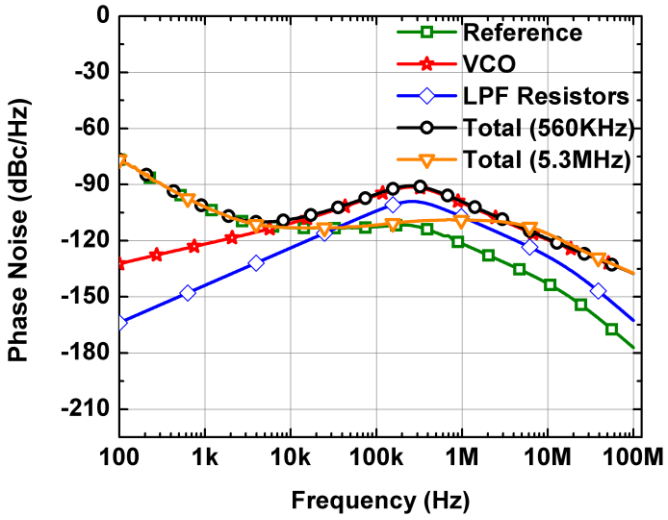

Figure 33. Simulated results of the PLL phase noise using pure frequency multiplied crustal oscillator (GMXO-FR). (Curtesy of Winzel Associates).

Figure 33 also includes the simulated phase noise of the PLL with higher loop bandwidth, and clearly shows the phase noise improvement by increasing the bandwidth using this pure reference clock.

The output power of the PLL was measured using an Erickson PM2 calorimeter.

One of the differential outputs of the PLL was terminated on-chip to facilitate measurement. Extra 3 dB was added to measured data to account for differential output power. The losses of the probe and waveguide connections were accurately measured using the PNA with D-band extender modules and de-embedded from the power measurement. In addition, the small losses from the D-band to W-band waveguide taper, as well as the extra WR-10 waveguide section used in the calorimeter, was de-embedded using the measured data provided from the VDi company. Figure 34 shows the measured output power across the locking range of the PLL.

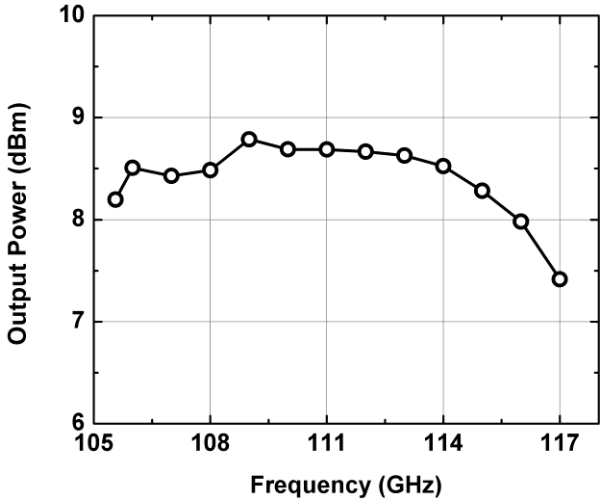

Figure 34. Measured output power of the PLL across the frequency at nominal biasing conditions.

The average output power is greater than +8 dBm across the frequency under nominal biasing conditions. In addition, the generated power is relatively flat across the frequency, which is the result of the wideband matching network design at the output of the VCO. Utilizing the coupled VCO topology allows full utilization of the generated power from the VCO and results in higher output power from the PLL. This PLL can be used in FMCW radar applications without an additional PA, which can save DC power and

reduce design complexity. In addition, high output power is advantageous for LO distribution networks in larger system designs.

Table 2-Performance summary of the PLL compared to state-of-the-art.

Reference	[20]	[25]	[28]	[26]	[18]	[27]	[24]	**This work**
Frequency (GHz)	122.7-122.9	132.1-132.6	92.7-100.2	158	80-100 160-169	93.4-104.8	156	**105-117**
Locking range (%)			7.8	2.8	22.2 5.5	11.5%	10.8%	**10.8%**
Reference frequency	60 MHz	259 MHz	1.5 GHz	130 MHz	5.62 GHz	100 MHz	900 MHz	**457MHz**
Phase noise (dBc/Hz) @ 100KHz	-60.1 @ 10 KHz	-	-92.5	-80.54	-93@ 90 GHz -88@ 162 GHz	-65	-	**-79**
Phase noise (dBc/Hz) @ 1MHz	-	-77.2	-102	-85	-100 @ 90 GHz -97 @ 162 GHz	-86.1	-89	**-100**
Phase noise (dBc/Hz) @ 10 MHz	-99.5	-	-105.5	-	-105@ 90 GHz -99.7@ 162 GHz	-103.5	-	**-121**
Output power (dBm)	-21.9	-	+3	-19	-3 @ 90 GHz -25 @ 163 GHz	-	-9	**+8**
PDC (mW)	87.7	120.8	469.3	24	1200	57	360	**600**
Technology	65 nm CMOS	65 nm CMOS	130 nm SiGe	65 nm CMOS	130 nm SiGe	65 nm CMOS	130 nm SiGe	**130 nm SiGe**
Chip area (mm^2)	1.09	0.88	0.93	0.96	1.1 ×1.7	0.88	0.293	**1.5 ×1.4**

Table 2 summarizes the performance of this design compared to the published state-of-the-art. The present design achieves comparable performance with the highest output power and the best phase noise performance at higher offset frequencies from the carrier.

CHAPTER 3. PHASE-LOCKED SUB-MMW RADIATOR DESIGN

3.1 Motivation

Signal sources are important part of electronic systems including Radars, wired and wireless communication transceivers, sensors, central processing units (CPU) and any other types of systems that require stable and low noise timing sources or RF signals for communication, ranging and detection. Designing on-chip signal sources in silicon technologies with low phase noise, high output power and wide tuning range is challenging at mmW and sub-mmW frequencies. On-chip sources however, can significantly reduce the complexity and packaging challenges of mmW systems. At Terahertz frequencies, low phase noise signal sources which can deliver adequate output power are essential components of envisioned Terahertz (THz) systems, since the signal source strongly impacts the overall performance of the entire system. In transmitter side, the generated RF power directly affects the length of the communication link. In the receiver side, the power of the LO significantly affect the sensitivity of the down-conversion mixers and thus receiver. However, generating high signal power at Terahertz frequencies using the current silicon technologies is very challenging.

Sub-mmW fundamental sources have been implemented in III-V technologies. [100]. By increasing the speed of silicon technologies, there have been attempts to generate RF power at higher mmW and sub-mmW frequencies. These approaches mainly rely on harmonic generation techniques either from harmonic oscillators [32],[34],[78] or

frequency multipliers [28], [90], [101], [102]. The reported circuits mainly suffer from low output power, poor phase noise and insufficient tuning range.

Arrays and phased-arrays are elegant solutions that have been used to boost the performance of electronic systems and to add the possibility of electronic beam steering at the cost of DC consumption and design complexity. Similar technique has been used recently to combine the output power of several signal sources beyond mmW frequencies [33], [37], [103]. However, the frequency and phase of the signal sources should be synchronized in this approach. The reported arrays, normally rely on injection-locking technique for synchronization which only provides limited locking-range. To utilize this technique in practical applications, adequate locking-range is required.

In this chapter, the design of high performance mmW and Terahertz signal sources will be studied first. A novel technique was proposed for phase locking free running signal sources with strong locking condition and wide locking-range across the entire tuning range of the VCOs. A 2×2 array which utilizes on-chip antennas was demonstrated as a proof of concept that can generate around 0 dBm at frequencies above the f_T of the utilized technology. The array generates and radiates Terahertz signal at the same time. The power of the locked signal sources was spatially combined in free space to produce more power. This work was further extended by including a PLL in the system which locks the phase of the entire phase-locked array into the phase of stable crystal oscillator. The proposed technique in this study can be utilized to phase-lock any type of oscillator topologies. In addition, the proposed architecture is scalable in 2D dimension for generating high power signals at Terahertz frequencies.

3.2 Low Phase Noise and High Output Power Signal Sources

Measured results of two monolithic signal sources which were implemented in a 130 nm SiGe HBT BiCMOS platform are reported in this section. One oscillator was designed to produce a signal at 367 GHz using a push-push topology, and another fundamental frequency oscillator was designed at 154 GHz. The 130nm ihp SG13G2 SiGe BiCMOS platform was used for these designs. This technology provides SiGe HBTs with an f_T and f_{max} of 300 and 450 GHz, respectively. The 367 GHz oscillator presented out-performs previous silicon-based implementations in terms of phase noise (and is competitive with existing III-V sources) and provides high output power with low DC power consumption.

3.2.1 Circuit design

Push-push oscillators have the advantage of compact size and low power consumption over multiplier-based implementations. It also provides a virtual GND on the fundamental signal at the push-push node and automatically suppresses the fundamental signal at the output. Since large transceiver arrays are often the desirable solution for many Terahertz applications, it is critical to have compact size and low power consumption. Figure 35 shows the schematic of the push-push oscillator. This oscillator utilizes a differential Colpitts topology and the second harmonic of the generated signal is extracted as the output. Any common node in this circuit can be used to extract the even harmonics where the fundamental signal is suppressed, while two out of phase fundamental signals are added destructively. However, simulation results show that the common-base node enables higher output power when the collector connections are AC shorted to ground.

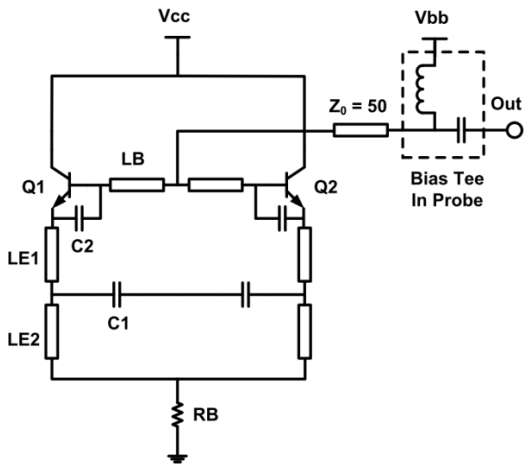

Figure 35. Schematic of 367 GHz Colpitts push-push oscillator.

An important consideration in designing submillimeter-wave circuits comes from the effects of VIA connections. Since the size of required inductors are very small and comparable with the magnitude of the parasitic inductances created by VIA stacks, it is important to include the VIA stacks in the EM simulations. In particular, the losses introduced with the VIA connections degrade the speed of transistors and Q of resonators. Any Q degradation increases the phase noise and reduces the generated power. As an example, Figure 36 shows EM simulation results highlighting the effects of VIAs on the Q of the base inductor.

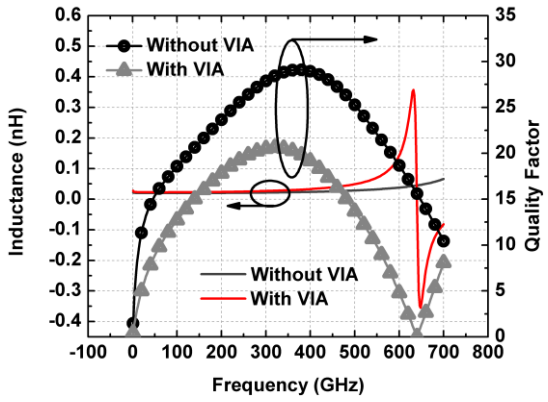

Figure 36. Effects of VIA connections on the Q of base inductance.

The current SiGe push-push oscillator was designed to oscillate around 180 GHz in order to provide the second harmonic signal at 360 GHz. All the inductors in the circuit were realized using microstrip lines which were fully EM simulated. This technology provides 3 μm thick aluminum for top metal interconnections and this layer was used as the signal trace in the microstrip transmission lines. Small metal-insulator-metal (MIM) capacitors present in this SiGe platform were used to implement the capacitors in the circuit and were also EM simulated together with the microstrip lines. In addition, the layout of the circuit was systematically optimized to avoid unintended couplings between the components and to maintain a symmetric layout to effectively suppress the fundamental signal at the push-push output node.

The 154 GHz signal source was designed to create the high output power needed in many transceiver implementations. The 154 GHz oscillator utilizes a similar topology to the schematic of the VCO in Figure 6, except, it utilizes the MiM capacitors instead of varactors. The cascode topology provides isolation between the oscillator core and the load, in addition, it can provide higher output power due to the increased breakdown voltage of the cascode devices because of small base impedance. However, it slightly degrades the phase noise performance of the VCO. The 154 GHz oscillator provides a differential output signal, however, in order to be compatible with measurement setup, one of the outputs was terminated on-chip and the other one routed to the output pad.

Quarter-wave transmission lines were utilized to provide DC biasing for the collectors of cascode devices. Metal 2 was used as a GND plane for both of the designs, which enables M1 interconnection for use as supply lines while remaining transparent to the high frequency signal lines. The skin depth at these frequencies is low, thus, the thin

1µm Metal 2 is sufficient for the GND plane with no need to combine several metallization layers to make a low loss GND plane. The output PADs were kept small to reduce parasitic capacitance and were designed and fully EM simulated to eliminate any unintended mode propagation at the desired frequencies.

3.2.2 Measured Results

A custom measurement setup was utilized, which was using a WR2.8 EHM harmonic mixer from VDi. The mixer was directly connected to high frequency waveguide probe. Figure 37 shows the measured signal and Figure 38 shows the phase noise of the 367 GHz push-push oscillator after being downconverted with a 20th harmonic mixer with LO frequency of 18.306 GHz. To identify the downconverted signal, the LO frequency was shifted slightly. Since the mixer utilizes the 20th harmonic for downconversion, this results in a 20X shift in frequency on the downconverted desired signal. Thus, the desired tone can be easily identified.

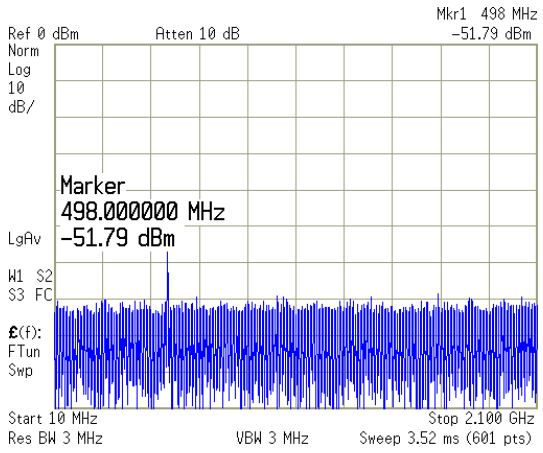

Figure 37. Measured frequency spectrum of the 367 GHz source after downconversion with 20th harmonic mixer.

The measured phase noise of this 367 GHz oscillator was -110.8 dBc/Hz at 10 MHz offset from carrier which is the best phase noise among the reported signal sources in silicon and at this frequency range. Table 3 shows benchmarking comparisons and indicates that this oscillator achieves a FoM close to [102], which has used an external low phase noise signal as an input to the multiplier (and is, hence, not a completely fair comparison).

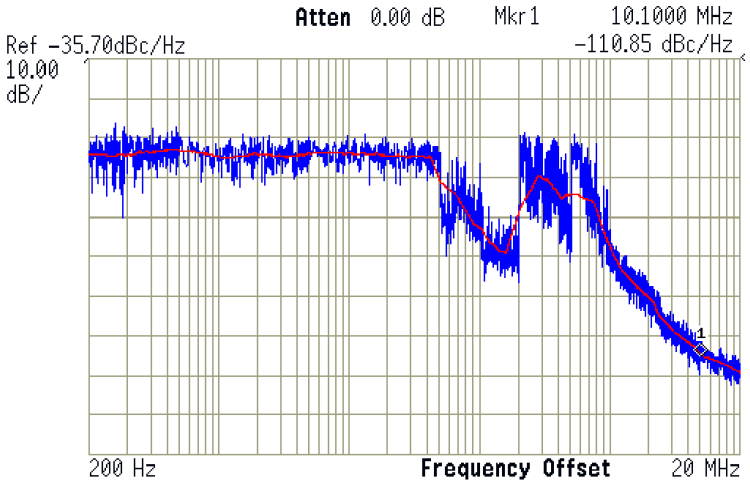

Figure 38. Measured phase noise of the 367 GHz source after downconversion with 20th harmonic mixer.

Because of the extensive EM simulations utilized and careful layout design, the measured fundamental frequency is within 2% of simulation. The output power of this signal source was estimated by considering the loss of the probe and the conversion loss of the WR2.8 EHM mixer based on the measured data provided by the company.

The measured output power is -8 dBm and the circuit draws 20 mA from a 3.2 V supply. Since the reported conversion loss of the mixer has been measured under 50 ohm matched conditions, the conversion loss of the mixer in this case should even be higher and hence the actual value of the output power should be more than -8 dBm. The DC power

consumption of the current design could be reduced further without substantial performance loss if a smaller resistor was used in the tail current bias.

The measurement of the 154 GHz oscillator was carried out by utilizing D-Band frequency extenders from OML. The OML extenders were used as a harmonic mixer to downconvert the 154 GHz signal to a low IF frequency. To accomplish this, an external LO signal was applied to the frequency extender and the output from IF port was collected and imported to the spectrum analyzer.

Figure 39 shows the downconverted signal using the 10th harmonic of the 15.338 GHz LO signal. Figure 40 shows the phase noise response of this oscillator, which achieves -87 dBc/Hz at 1 MHz offset frequency from carrier.

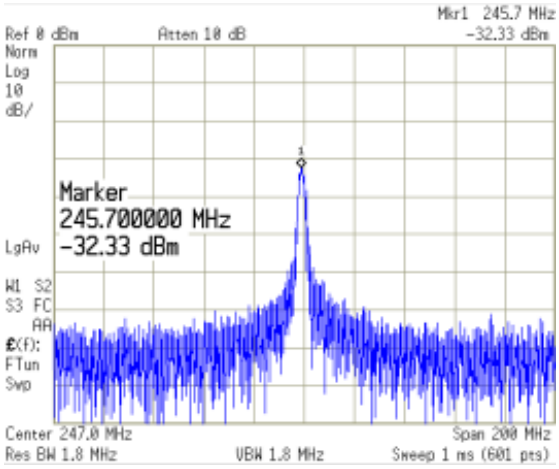

Figure 39. Measured frequency spectrum of the 154 GHz signal after downconversion with a 10th harmonic OML T/R.

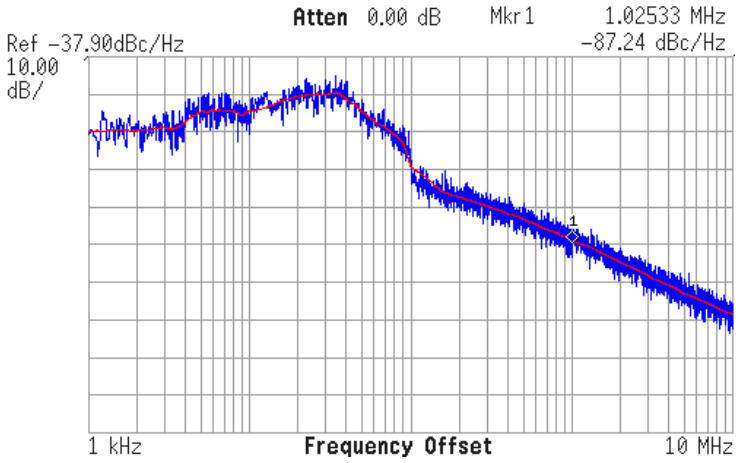

Figure 40. Measured phase noise and of the 154 GHz signal after downconversion with a 10th harmonic OML T/R.

The measured output power of this 154 GHz source is 7 dBm (differential), which matches well with simulations, and this signal source draws 17 mA of current from a 4 V supply. The output power of this source was measured by comparing it with a reference source with a known output power. The reference signal was applied to the same OML module in the same configuration as the 154 GHz signal source. The other OML T/R module was used as a reference source, by utilizing the terminated reflective load. Therefore, two OML modules were utilized. One module serves as the reference signal source at D-band and the other module serves as the down conversion receiver module. Since the generated power from the reference OML module was known, by watching the IF port of the down-conversion T/R, one can easily calculate the conversion loss of the receiver. The extra path loss including the probes and waveguides were also calibrated and de-embedded properly.

The performance of this signal source is compared with published state-of-the-art data in Table 3. A well-known FoM is used in the table to compare the signal sources, in terms of phase noise and DC power consumption (a more negative number is better). The die micrographs of both circuits are shown in Figure 41.

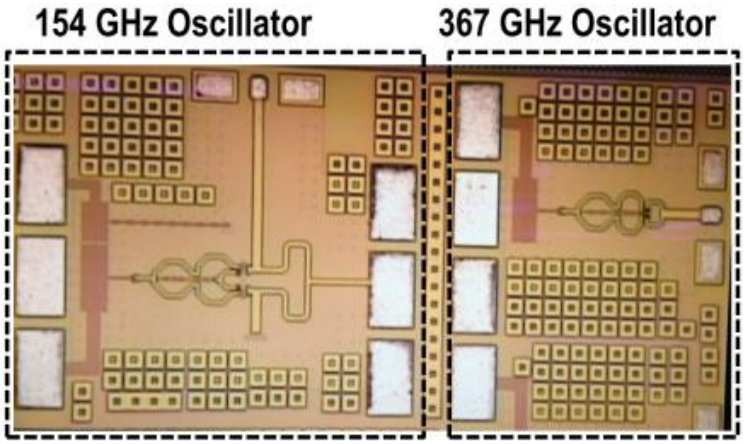

Figure 41. Die micrographs of the fabricated oscillators (the 367 GHz circuit is 0.2 mm2 and the 154 GHz circuit is 0.37 mm^2).

Table 3. Measurement summary and comparison with the state-of-the-art.

Ref	Frequency (GHz)	Phase Noise (dBc/Hz)	Output Power (dBm)	DC Power (mW)	Topology	FoM	Platform
[32]	320	-77 @ 1MHz	-3.3	339	Cross-Coupled	-161.8	65 nm CMOS
[90]	309-330 288-311	-78 @ 10MHz -102 @ 10MHz	-13.3 -1.7	63 167	Push-push Doubler	-150.4 -169.2	120 nm SiGe
[100]	310 346 287	- - -97 @ 10MHz	-6.2 -11	76 115 78	Series Tuned Series Tuned Series Tuned	- - -166.8	256 nm InP DHBT
[102]	325	-101 @ 1MHz**	-3	420	Multiplier Chain	-185.0	130 nm SiGe
This Work	**367**	**-110 @ 10MHz**	**-8**	**64**	**Push-Push Colpitts**	**-183.3**	**130 nm SiGe**
[104]	136-150	-87 @ 1MHz	2-3	154	Colpitts	-168.6	SiGe
[105]	145-158	-86 @ 1MHz	3	68	Colpitts	-171.6	SiGe
[106]	157-165	-79 @ 0.5MHz	-15	47	Colpitts	-172.2	130 nm SiGe
This Work	**154**	**-87.2 @ 1MHz**	**+7**	**68**	**Colpitts**	**-172.6**	**130 nm SiGe**

3.3 A 2×2, SiGe Scalable Transmitter Array

Several approaches have been reported recently to create RF power at frequencies beyond the peak f_T of the transistors. Power combining techniques have been utilized traditionally to combine the output of several amplifiers to produce more RF power. One solution is to use a central signal source with multiple amplifier-multiplier units with a combiner (e.g., a Wilkinson combiner). The generated powers are inherently phase locked in this approach. However, such a design requires complex routings at extremely high frequencies, as well as high DC power consumption, and potential instability concerns, making this approach less desirable for the current design. On the other hand, any power combiner has a certain insertion loss associated with it, which limits the number of combinatory networks for very large array sizes. The other approach utilizes several local signal sources and combine the generated power to produce higher output power. To avoid the complexity and insertion loss of the power combing networks at such high frequencies, free space spatial power combing technique has been used in recently [37].

The main issue of the latter approach is the requirement for effective synchronization between the signal sources. If the signal sources were not frequency and phase-locked, even with very small phase or frequency deviations the resultant combined power will vary over the time with the rate equal to the difference in the frequency of the sources. At one instant, and in the certain point in space, the power will reach a peak value and then drop to zero as time evolves and changes the phase.

In [37], the signal sources are injection-locked to the central VCO to make a 4×4 radiating array at 280 GHz (and requires complex high frequency routing). Each cell of the

array itself contains a transmission line based ring oscillator to produce a strong 2nd harmonic content. The limited locking-range of the injection-locking approach, as well as its loose locking mechanism, may result in the locking failure in the presence of any frequency shift, due to process variations or any environmentally-induced deviation from the design frequency. Similar approaches have been reported which also utilize locked cross-coupled topologies with injection-locking technique [33],[103]. In the present work, a different locking methodology is proposed, to strongly lock the local signal sources together in a loop. A 2×2 transmitter array was designed and implemented as a proof of concept. The array utilizes 4 free running signal sources. These sources were strongly coupled to each other, while each source was radiating the generated RF signal through on-chip antennas. Since Colpitts oscillators out-perform other oscillator configurations at millimeter-wave frequencies, it is highly desired to find a way to lock these types of oscillators together for use in the array transmitters. It is shown in the present work, how this can be accomplished.

The push-push oscillator in Figure 35 was used as the core oscillator topology in the present design. This oscillator achieved a record signal purity among the other silicon-based oscillators at the relevant frequencies.

The proposed technique for phase locking the free running Colpitts oscillators is shown in Figure 42. A 2×2 array is shown here to show the concept, however there is no limitation on the array size, and the array can be scaled to any desired size in 2D dimension. The methodology relies on direct fundamental current injection between the neighbor oscillators to create phase locking conditions. Since the entire oscillation current is directly injected to the other oscillator, a strong coupling is created. In addition, the oscillators are

locked together in a loop, thus, each oscillator is being coupled to neighbor oscillators from two sides for stronger coupling.

This methodology can be explained in a simpler way by considering a differential Colpitts oscillator where two half branches are coupled together as shown in Figure 43. In fact, a differential Colpitts oscillator is an example of a simple network which only consists of two oscillators coupled together utilizing a similar coupling methodology. Each branch of the differential Colpitts oscillator is coupled to the neighbor branch of the neighbor oscillator, as seen in Figure 42 and Figure 44. This procedure is followed until the second

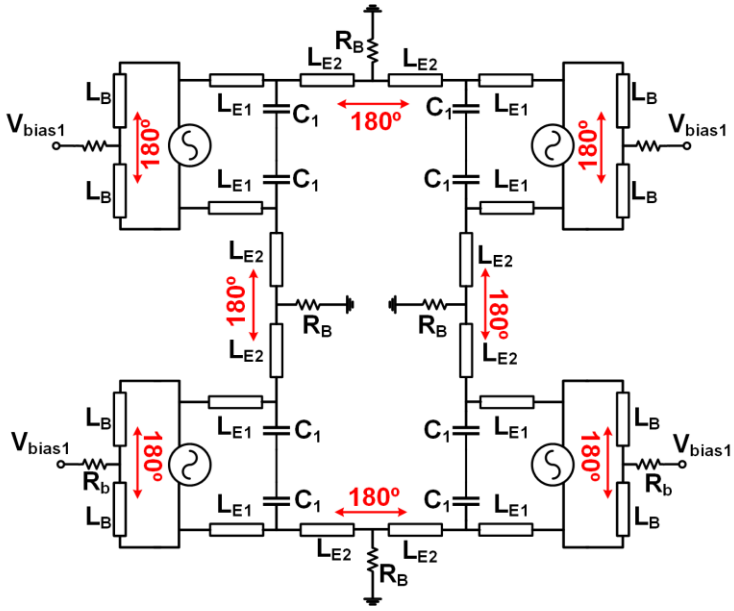

Figure 42. The block diagram of the proposed coupled 2×2 locked array.

branch of the last oscillator is coupled to the second branch of the first oscillator, to make a loop. The chain configuration utilized here, provides current injection from two sides of each oscillator to assure strong coupling within the network. The resistors at the common-node connections will effectively dampen any common-mode solution between two coupled branches. By inspecting this circuit, one can easily see the solution of the

single Colpitts oscillator is also a solution to this complicated oscillatory network. It can be shown that because of the generated loop, this solution is the only solution to this complex high-order system. These types of circuits with coupled oscillators can oscillate in different operational modes. It's important to assure the single mode operation of the system under any circumstance. The present circuit was designed in such a way to only excite the desired mode and to significantly dampen the other possible modes. For instance, the two left and right half-branches of the neighbor oscillators can oscillate either in a differential mode or in a common mode, each of which will enforce a different oscillation frequency to the entire network. In common-mode operation, each branch will oscillate exactly at the same frequency and phase as the other branch. While in differential mode, the two branches will have anti-phase oscillations at the same frequencies.

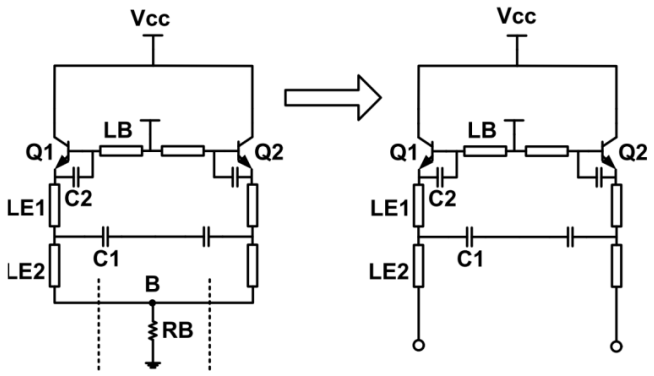

Figure 43. Breaking the oscillator circuit from its common node.

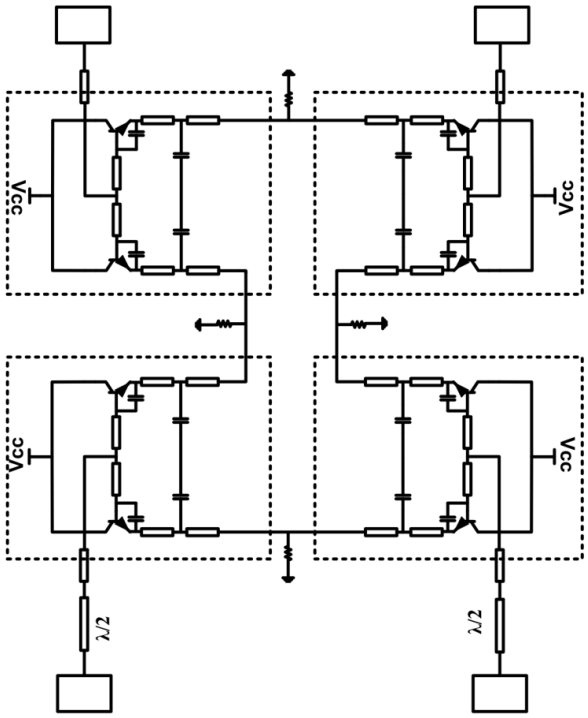

Figure 44. Proposed 2×2 phase-locked oscillatory array.

It was shown in section 2.2 that impedance looking from the emitter of Q1 and Q2 transistors determines the operational mode of the coupled VCOs. The T-network at emitter terminals of the Q1 and Q2 in Figure 35 was designed in such a way that only excite the differential mode (anti-phase coupling) and completely suppress the possibility of the common mode excitation. In addition, the losses introduced in the common nodes of the circuit will effectively dampen the common-mode and thus only the differential mode will survive.

The proposed locking mechanism which locally locks the neighbor oscillators together by injecting the entire oscillation current, can be used to lock any other oscillator topologies. The proposed technique, provides clear advantages compared to commonly used injection-locking technique which utilizes an external stable signal and distributes it

globally within the oscillatory network [37]. The first advantage of the proposed solution is the possibility of predicting the oscillation frequency by simply finding the oscillation frequency of the single oscillator cell, thus reducing the complexity of the design of this network to the design of single cell oscillator. The second advantage is its scalability to any larger 2-D array. The LE2 inductors in Figure 43 were utilized as the interconnections between the neighbor oscillators while serving as an inductor for the single oscillator cell. Since the oscillatory network will be placed inside the array of antennas, it is important to pay attention to the direction in which the circuit feeds the antennas so that radiation fields can combine constructively in the air. In the present layout, 180-degree phase shifter lines were added to the bottom cells, so that radiated power from the array combine in phase.

On-chip patch antennas were designed for this 2×2 transmitter array. This type of antenna automatically suppresses the surface wave excitation through the shielding GND plane. However, this type of antenna has a narrow bandwidth and the circuit needs to be carefully EM simulated to predict the oscillation frequency within the bandwidth of the antennas. The distance between the array elements is around λ/2. The dimensions and spacing of the antennas were optimized to get the maximum gain from the array network.

3.3.1 Measurement results

The proposed circuit was implemented in a SiGe HBT BiCMOS technology with the peak f_T and f_{max} of 300 GHz and 450 GHz, respectively (the IHP SG13G2 SiGe platform). This process technology has seven metal layers and the top layer has the thickness of 3 µm, which is suitable for high frequency transmission lines and antennas.

The silicon substrate has a thickness of around 300 µm. Figure 45 shows the die photo of the circuit which occupies 1.3×1.4 mm^2.

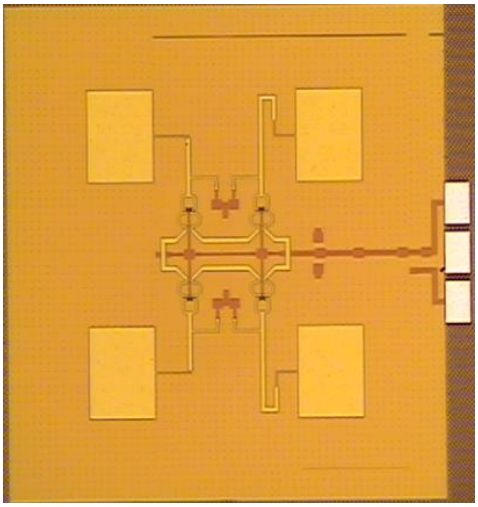

Figure 45. Die micrograph of the 2×2 array circuit.

In order to measure the radiated power and frequency of the transmitter, the die was mounted on a board and placed in front of the receiver. The receiver setup consists of a WR2.8 horn antenna with 26 dBi of gain and WR2.8 EHM mixer. The mixer is a 20^{th} harmonic mixer which down converts the received signal to the baseband. The distance between the receiver and the transmitter array was well in the far-field of the receiver antenna. To determine the far-field distance of the receiver antenna, the distance between the transmitter and receiver was varied between 120 mm to 155 mm. It was observed that the signal loss follows the predicted free-space path loss, meaning the transmitter was correctly placed in the far-field of the receiver antenna. Figure 46 shows the photo of the custom setup for measuring the frequency and power of the transmitted signal.

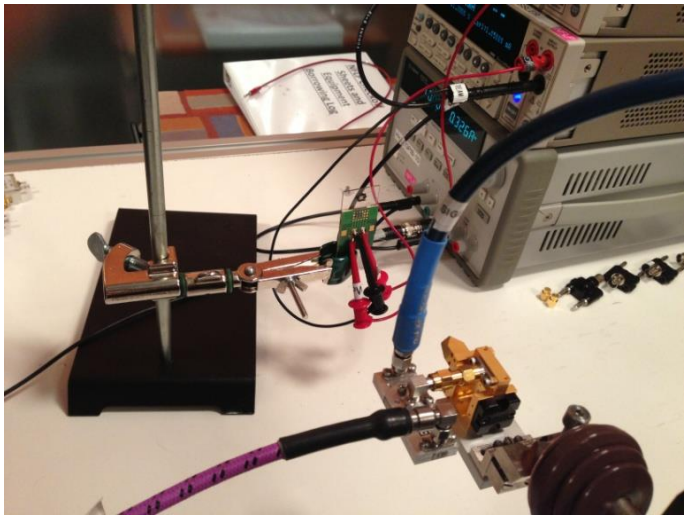

Figure 46. Measurement setup for detecting the transmitted signal.

The detected signal was amplified after down conversion with a 20th harmonic mixer and the detected IF signal is shown in Figure 47. The baseband amplifier provides around 24 dB of gain to the IF signal. The distance between the transmitter antenna and the receiver antenna was set to 155 mm for this data. Based on the power of the detected signal, and by

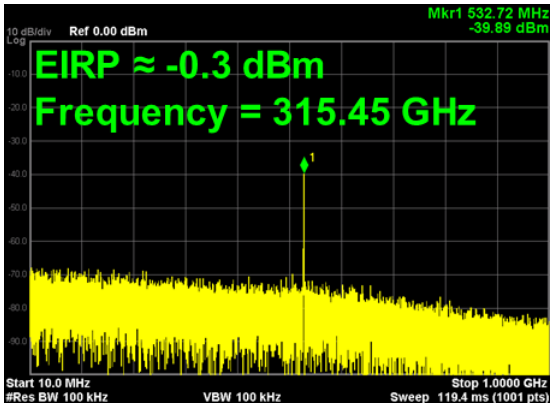

Figure 47. The spectrum of the detected signal after down conversion with a 20th harmonic mixer and base-band amplification.

calculating the free-space path loss as well as the loss of the receiver chain, the effective radiated power from the transmitter was predicted to be -0.3 dBm at 316 GHz. It is worth noting that the antennas were originally designed for 340 GHz and there is around

3 dB of gain loss because of the frequency shift of the transmitter circuit. More accurate EM simulations predict the oscillation frequency with less than 2% error.

Figure 48 shows the measurement setup and the measured radiation pattern of the antenna-array at 316 GHz. The gain was estimated by considering the mixer's conversion loss from the data sheet of the mixer. Absorbers were used for this measurement to absorb additional reflections. There is a small gain difference around zero degrees between the measured E-plane and H-plane which comes from the small misalignment between the horn antenna and transmitter array in the H-plane setup.

The performance of this array transmitter is compared with the state-of-the-art in Table 4. Considering the smaller array size and lower power consumption, this transmitter has the competitive performance.

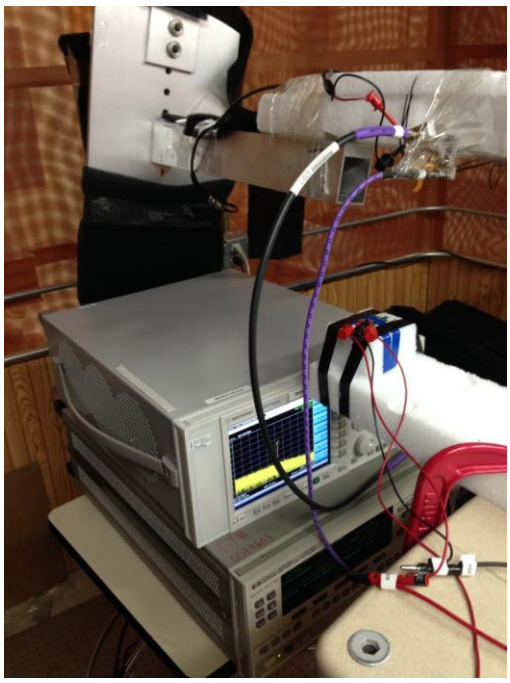

Figure 48. Setup for measuring the radiation pattern.

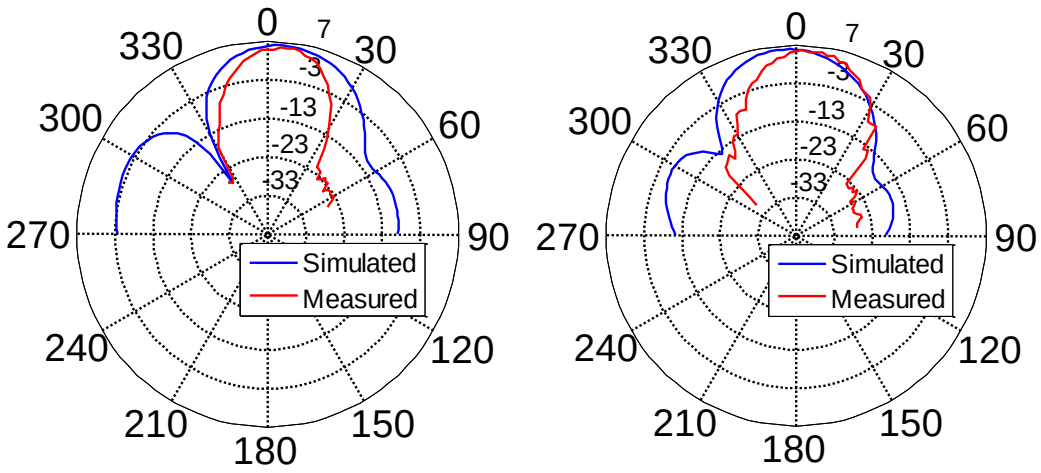

Figure 49. Measured H-plane compared to simulations (left). Measured E-plane compared to simulations (right). The measured E-plane was rotated 20 degrees for comparison purposes.

Table 4. Performance Summary Compared to State-of-the-Art.

Ref.	Frequency (GHz)	Radiated Power EIRP (dBm)	Array Size	DC Power consumption (mW)	Process
[107]	280	+9.4	4×4	820	45nm SOI CMOS
[28]	420	+3	2×4	700	45nm SOI CMOS
[31]	338	+17.1	4×4	1540	65nm CMOS
This work	**316**	**-0.3**	**2×2**	**225**	**130nm BiCMOS**

3.4 2×2 Locked Radiating Array at 230 GHz with on-chip PLL

A stable, low noise, well defined and controllable signal is necessary for any practical application, including communication and Radar systems. In addition, a stable and known signal tone can increase the dynamic range of the active imaging systems substantially. Since the illuminating signal is only a single tone in these types of imaging systems, and since the oscillation frequency is known, the IF bandwidth can be decreased substantially to lower the integrated noise content at the output of coherent imaging system while the signal power is not being affected. For all these reasons, a phase-locking to a stable crystal oscillator was necessary. In this section, a new technique is introduced for designing a frequency-doubler, and to boost the power of the second harmonic signal. In addition, a mechanism is demonstrated for locking the radiating array to a pure crystal by utilizing PLL. Furthermore, the locking technique proposed in section 0 was modified to systematically mitigate the possibility of the common mode excitation.

Frequency multipliers are extensively used for generating high frequency signals from low frequency signal sources. This approach has been utilized recently in generating mmW and Terahertz signal sources and PLLs [108],[102],[67],[29]. Any nonlinear circuit that can generate strong harmonic contents of the input signal, can be considered as frequency multiplier. The frequency multiplication can also be achieved by multiplying a signal by itself to create strong even harmonic contents of the input signal. Frequency doublers, or cascade of frequency doublers are widely used to provide high frequency mmW and Terahertz signal sources. Gilbert cell analog multiplier [26], push-push configuration [108], and nonlinear varactors [109] are the most common frequency doubler circuits that have been used in mmW systems. In this study, a combination of VCO and

frequency multiplier circuit is proposed as a small form factor circuit for generating strong second harmonic content at mmW and Terahertz frequencies. To understand the proposed concept let's first consider the widely used push-push topology shown in Figure 50. Other types of frequency multipliers have similar operational principal. The core of the circuit consists of transistors Q_M. This circuit requires differential input signals for proper operation which can be generated utilizing on-die Baluns or transformers at the expense of some power loss.

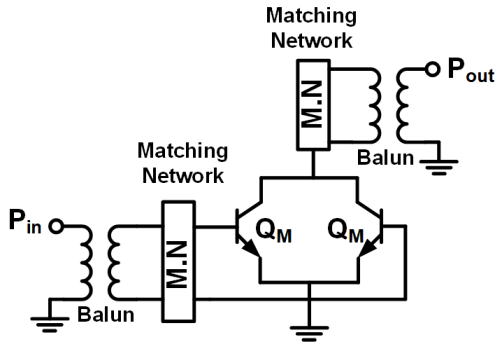

Figure 50. Schematic diagram of the push-push frequency doubler.

Since the input signal is differential, the fundamental harmonic and other odd harmonics of the input signal is suppressed at common collector connection at the output. However, the second harmonic and other even harmonics of the input signal would experience a same phase and add up at this node. When the input signal is not strong enough to switch the transistors, the common node connection at the output simply sums up the even harmonics of the input signal which are the result of nonlinear operation of transistors and suppresses the odd harmonics, assuming a reasonably good matching between the symmetric branches of the circuit. Thus, the second harmonic of the input signal can be extracted at the output. With stronger input signal, these transistors turn ON and OFF alternatively. At positive cycle of the input signal, the left transistor turns ON and at negative cycle, the right transistor turns ON. Due to symmetricity of the circuit, it is

effectively switching 2 times in each cycle of the input signal, and effectively creates a waveform at twice the frequency of the input signal. However, for the optimum power generation, input and output matching networks are needed as well as reflectors of the first and second harmonics at output and input of transistors respectively. (see [108] for more details about this circuit topology). The required input and output Baluns, matching network and reflectors can significantly increase the layout area and increase the insertion loss. The spacing of the antennas in phased array circuits are designed for efficient far filed combination, and maximum gain. The area between the antennas are fixed and is around $\frac{\lambda}{2}$ for the maximum array gain. This area limitation, sets a significantly challenging boundary to the layout area of the array circuits. Thus, reducing the layout area of the standalone cells is highly desirable. An alternative solution for saving the layout area is to use push-push oscillator topology [10]. The presented circuit in previous section (see section 3.3, Figure 43), has utilized push-push oscillator configuration to create a signal at 316 GHz. The main drawback of using push-push topology comes from the lower isolation between the oscillator core and 2nd harmonic node which can impact the generated power and phase noise in the presence of strong 2nd harmonic content. However, the generated power using frequency multipliers can be higher than push-push oscillators if properly designed. Nevertheless, both configurations have been widely used in literature.

Because of the availability of on-chip signal source in the present design, a more efficient topology is proposed here to increase the output power and reduce the footprint of the circuit at the same time. The proposed technique essentially utilizes a combination of the above approaches to provide more output power while preserving higher isolation between the oscillator core and the frequency multiplier. Figure 51 reproduces the

schematic of the Colpitts topology from previous section. The circuit generates high frequency signal and pumps the generated current to the output of the oscillator using Q1 and Q2 transistors. The output port is isolated from the resonator core because of collector-base isolation of the Q1 and Q2 transistors. Because of this reasonable isolation, the load at the output of the oscillator does not impact the operation of oscillator significantly, thus the oscillator core can effectively be considered as a mmW current source. Although the C_{CB} capacitance can effectively decrease this isolation, a cross-coupled dummy C_{CB} capacitance can effectively cancel the effect of C_{CB} capacitance if needed [110]. Using this concept, a current mode frequency multiplier is proposed for efficient frequency multiplication, to avoid input matching network and to reduce the DC power consumption and layout area. Figure 52, shows the proposed current mode frequency multiplier. The input RF signal is pumped into emitter terminals of the multiplier and the second harmonic is extracted from the common collector node.

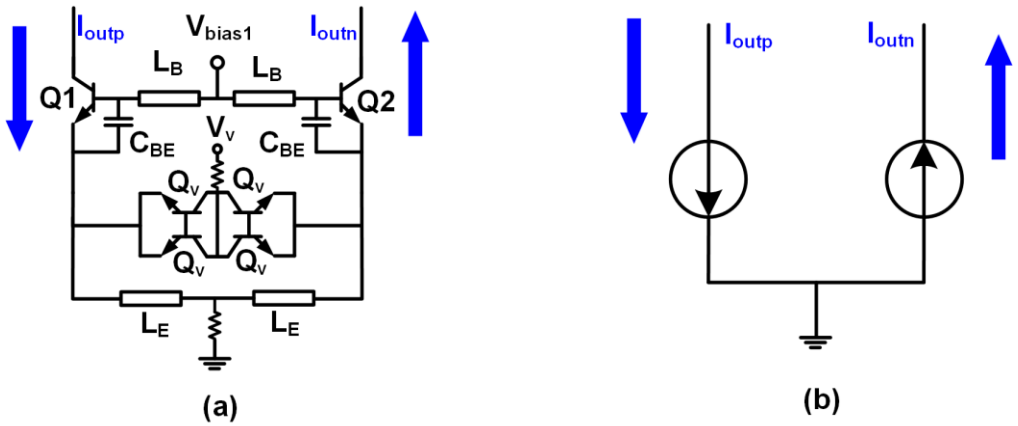

Figure 51. Schematic diagram of the Colpitts VCO (left). Current source representation of the isolated VCO (right).

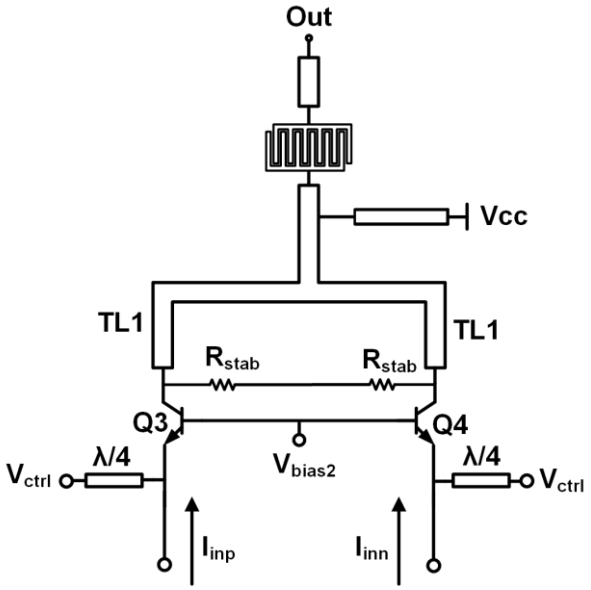

Figure 52. Schematic diagram of the proposed current mode frequency doubler.

Because of low impedance of emitter terminals, it will automatically absorb the entire input mmW current from the oscillator core without a need for any matching network. In addition, the input Balun can be omitted since the VCO core provides balanced current signals. This frequency multiplier operates as current rectifier to produce a strong second harmonic content at the output. Thus, it would be advantageous if the conduction angle of the transistors can be controlled to further increase the 2nd harmonic content at the output. Quarter-wave stubs were designed at fundamental frequency to force the DC voltage of the emitter terminals while the base voltage is also tied to another bias voltage. By applying V_{ctrl}, the conduction angle of the multiplier transistors can be controlled. These $\frac{\lambda}{4}$ stubs present high impedance at fundamental frequency and does not impact the operation of the VCO core. Furthermore, these stubs act as $\frac{\lambda}{2}$ line at 2nd harmonic frequency and provide very small impedance at 2nd harmonic frequency which operate as reflectors of the 2nd harmonic signal. This stub, not only could increase the 2nd harmonic content at the

output, it also increases the isolation of the multiplier output from the VCO core, and eliminates any phase noise degradation due to flicker noise up-conversion as a result of second harmonic signal [111]. The increased isolation also helps the design of the output matching network of the multiplier which can be optimized independent of the VCO core.

Figure 51 and Figure 52 suggest that proposed multiplier can easily be cascaded on top of the Colpitts core to reuse the biasing current and further reduce the layout area. Figure 53 shows the complete schematic of the VCO-frequency multiplier topology. Contrary to push-push oscillators, where the differential outputs of the oscillators are immediately tied together to suppress the fundamental signals, strong fundamental signals are still existed at the collector terminals of the QM transistors as well as TL1 lines. Presence of these signals can potentially cause stability problems. Additional R_{stab} resistors were designed to properly attenuate these fundamental signals.

Figure 54 shows the simulated output power of the VCO-Multiplier combo circuit across the tuning range of the VCO. The generated average output power is above +2.2 dBm with the peak output power of +4.9 dBm at 240 GHz. The combo circuit can be viewed as an oscillator which directly provides high output power at 2^{nd} harmonic of the designed VCO. To simulate the improvement in output power by reducing the conduction angle, Figure 55 shows the simulated output power versus the applied V_{BE} voltage. Controlling the conduction angle improves the output power considerably.

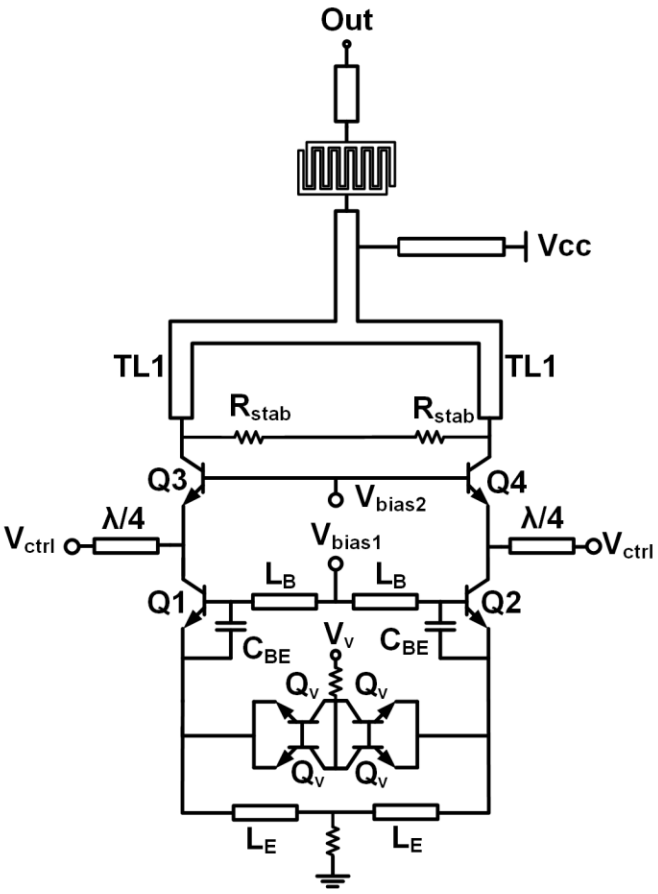

Figure 53. Schematic diagram of the proposed VCO-frequency doubler.

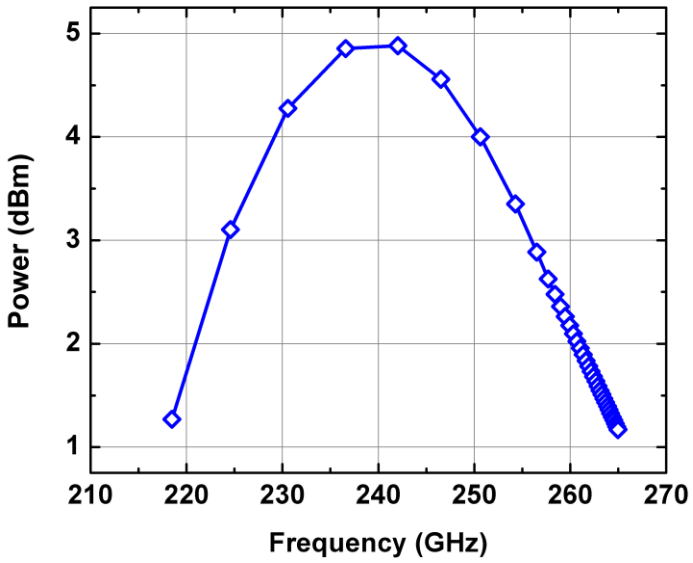

Figure 54. Simulated output power of the VCO-multiplier combo circuit.

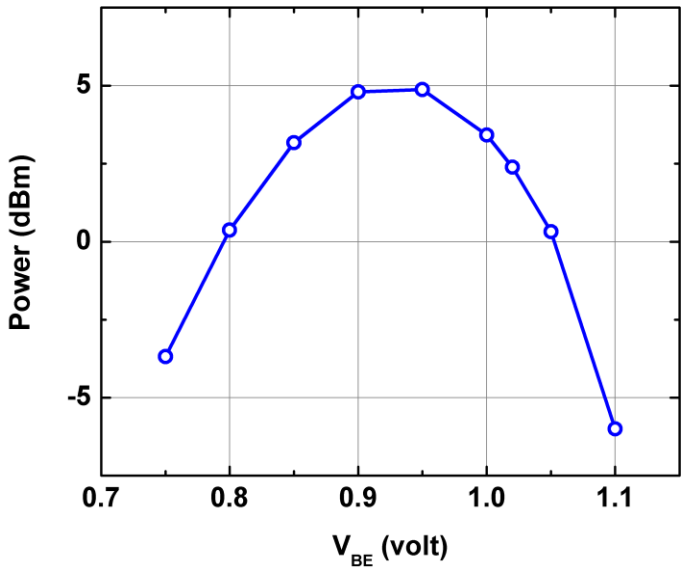

Figure 55. Simulation result showing the dependence of the output power of the VCO-multiplier combo circuit to conduction angle of the transistors.

To phase lock the VCO-multiplier combo circuit, a similar approach as in section 3.3 can be utilized. The VCO cores can be phase-locked using the combination of LB, LE and varactors to inject the fundamental oscillation currents for strong coupling. The main difference of the proposed technique comes from the fact that these VCOs are not just simply coupled to each other, they share components with the neighbor VCOs, thus, not any single oscillator can oscillate without its neighbor VCO. Therefore, the entire network operates as single oscillator and prevents simultaneous excitation of the oscillation modes if existed and effectively mitigates the possibility of any chaos in bigger array circuits. In addition, the coupling technique in the current section was modified to mitigate the multimodal excitation problem existed in previous topology. This allows more flexibility in designing emitter impedances for better tuning range and phase noise rather than designing for mode suppression. The emitter inductance in this new scheme can improve the tuning range of the VCOs by resonating with the parasitic capacitance at emitter node.

Thus, nearby VCOs were designed to couple in differential mode. Figure 56 shows the modified locking technique to phase lock the free running Colpitts VCOs. The modified technique, utilizes the fundamental current injection through base inductors and varactors as well as emitter T-lines to establish strong coupling between the neighbor VCOs.

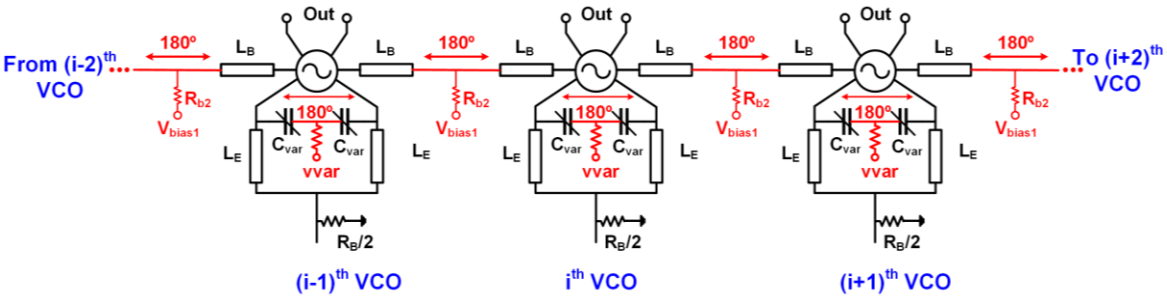

Figure 56. Block diagram of the modified differential phase locking scheme.

The common mode damping can now easily be accomplished by only adding the resistors at common nodes. The added loss does not impact the differential operation, since the common nodes are virtually grounded in differential mode. However, these resistors directly appear in the common mode oscillation path, thus can mitigate the possibility of common mode oscillation. The biasing resistors at common node emitter connections in Figure 44, cannot mitigate the excitation of common modes between the coupled neighbor oscillators. Since these nodes will be open circuit in common mode operation, thus we had to specifically design the emitter impedance to drastically reduce the negative resistance of the oscillator feedback path in common mode operation. This limits the flexibility in optimizing the performance of the VCOs for tuning range and phase noise. This problem is completely mitigated by utilizing the modified technique shown in Figure 56.

The next step is to lock the phase of the entire locked array to an external highly stable crystal oscillator. Locking a free running VCO to low frequency crystal oscillators

is traditionally accomplished by utilizing a PLL. The same technique was used in this study to phase lock the radiating array to external crystal reference signal. The D-band PLL from CHAPTER 2 was used for this purpose. The VCOs in array core were designed to oscillate at the same frequency range as the D-band PLL. One challenging problem comes from the layout and routing the differential LO signals across the circuits in mmW and sub-mmW systems. To utilize the PLL loop we must sample a differential signal from the locked array and divide the frequency to the frequency of the external crystal for comparison and making the PLL loop. It was shown in section 2.3.1 that locking range of mmW frequency dividers are strongly depend on the injected input power, thus it is important to drive the frequency dividers with adequate signal power to avoid limiting the locking range of the PLL loop. A similar approach which was presented earlier in CHAPTER 2 was used in the current study as well. An extra D-band VCO was designed without frequency multiplier. This VCO was also phase-locked inside the radiating array circuit. This VCO provides extra power port for driving frequency dividers with high power to assure wide locking range without sacrificing the signal power from radiating cells. The output of the interface VCO was matched to the input of the first frequency divider to assure adequate power delivery. The block diagram of the proposed array including the interface VCO for driving frequency dividers is shown in Figure 57. The varactor terminals of the standalone VCOs are all tied together, and the PLL loop controls this node for locking the frequency and phase of the free running VCOs to a crystal reference.

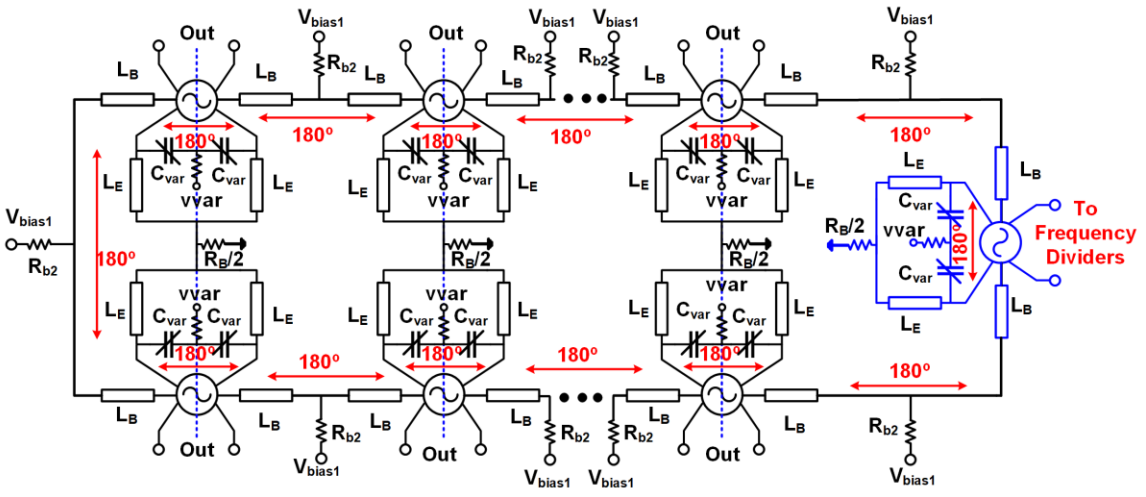

Figure 57. The block diagram of the locked array including the extra VCO for frequency divider interface.

On-chip Bow-Tie slot antennas were designed to radiate the generated signal from the output of the frequency doublers. These antennas were designed to radiate from the backside of the chip and through silicon. Compared to previously designed patch antennas in section 3.3, these antennas provide much wider bandwidth but, with reduced gain. Since on-die signal sources with limited tuning range were used in this design, the antennas should be sufficiently wideband to efficiently radiate in the presence of any frequency shift. Due to big difference on refractive indices of silicon and air, considerable portion of the radiated wave may bounce back at silicon-air boundary. It is important to assure that silicon thickness is thin enough to prevent the generation of standing waves inside the silicon. Alternatively, silicon lenses can be used to radiate most of the waves off the silicon into the air. Utilizing Silicon lenses can increase the radiation efficiency, directivity and gain, but increases the packaging complexity.

A 2×2 array was implemented as a proof of concept, in ihp's 130-nm SiGe technology. Die photo micrograph of the fabricated chip is shown in Figure 58. Figure 59 shows the schematic diagram of the circuit including the high-power interface for driving the frequency dividers. The PLL part was omitted in this figure for simplicity. The details of the PLL design can be found in CHAPTER 2.

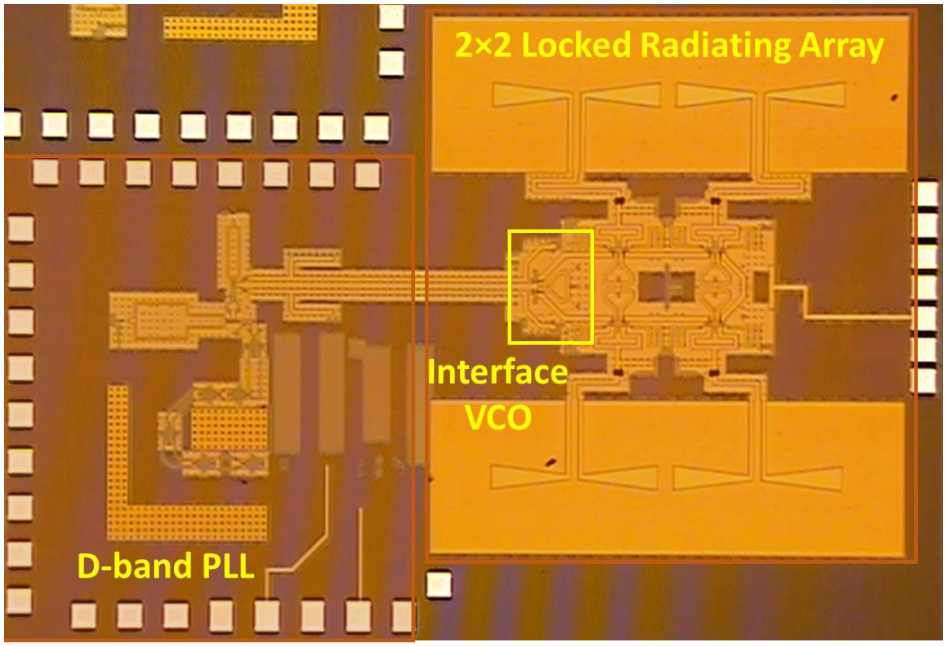

Figure 58. Die photo of the 2×2 radiating locked array.

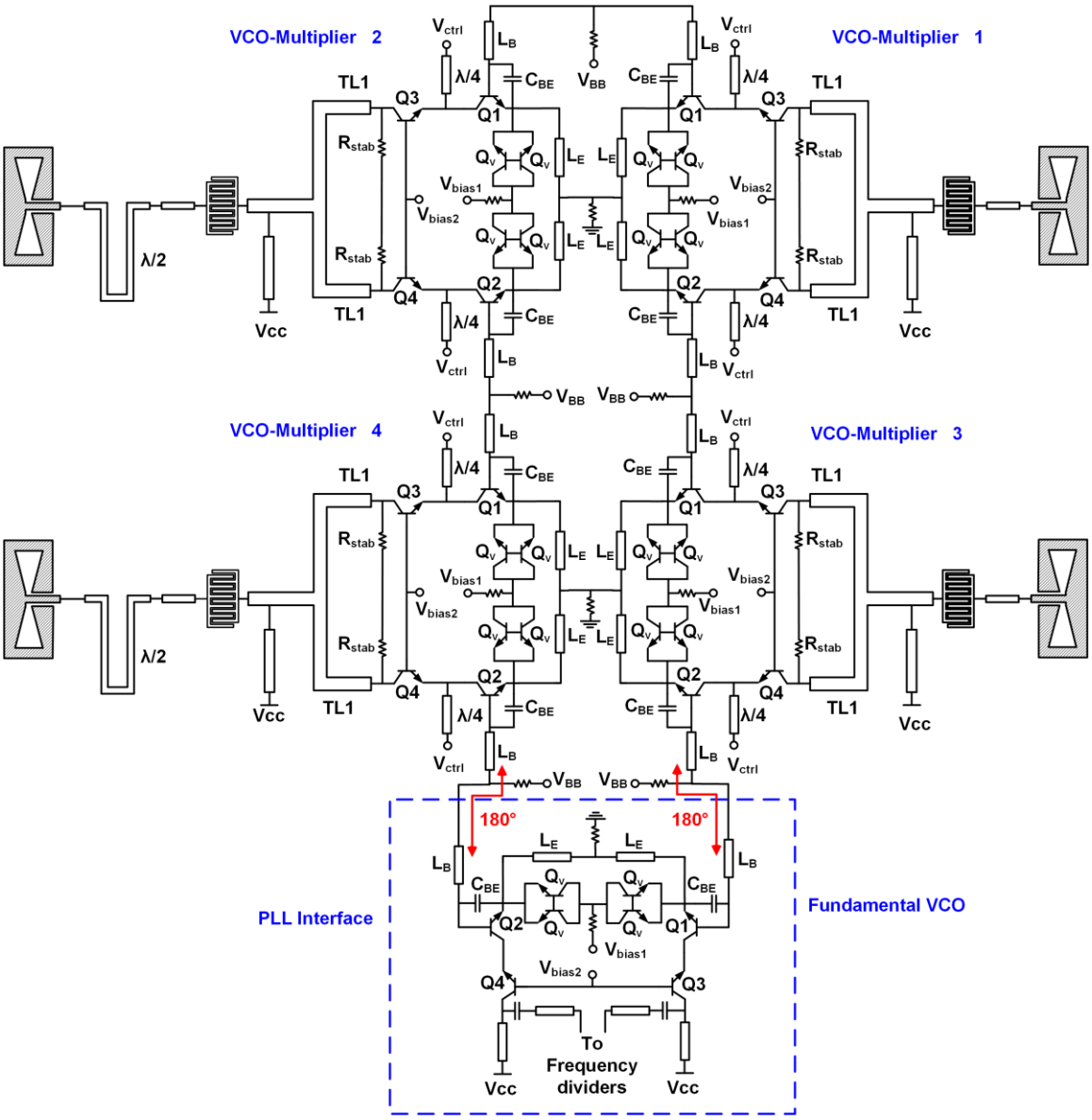

Figure 59. Schematic diagram of the 2×2 radiating array, including the frequency divider interface.

CHAPTER 4. MILLIMETER-WAVE AND SUB-MILLIMETER-WAVE FULLY INTEGRATED TRANSCEIVERS

4.1 Motivation

Advances in silicon technology has enabled the serious possibility of implementing of millimeter-wave (mmW) and terahertz (THz) circuits on silicon. There are several applications that can benefit from the integration and reliability capabilities of silicon, including: broadband communications, high resolution ranging, imaging, chip-to-chip communication, spectroscopy, security and radiometry. However, the implementation of the high-performance circuit and systems remains challenging at mmW and Terahertz frequencies. The fundamental challenge comes from the high path loss at those frequencies, high NF_{min} and limited f_{max} of the devices. Thus, generating adequate power at those frequencies, in current technologies is challenging. In addition, due to limited f_T of the devices, the minimum achievable noise figure is still high which reduces the sensitivity of the receivers at these frequencies. Furthermore, at frequencies close to f_T of the devices, the transistors cannot provide adequate power gain, thus, most of the reported circuits utilize direct detection or conversion of the received signal without amplification at RF frequencies. High performance and low noise THz circuits are conventionally realized using Schottky diodes with discrete waveguides at sub-mmW frequencies [39], [38]. This type of approach can achieve high performance, but is not suitable for large-scale manufacturing because of the large sizes and complexity involved. In [43], 220 and 320 GHz receiver front-ends were demonstrated using SiGe HBTs, where the 320 GHz receiver employs an integrated ×9 multiplier to provide the LO signal for a sub-harmonic mixer to

downconvert the incoming RF signal. The receiver achieves 36 dB single-side-band (SSB) NF. The integrated multiplier chain draws 600 mA from a 5 V supply. In [31], a 380 GHz transceiver is reported which uses quadrupler and on-chip signal source for the transmitter. The reported EIRP of the transmitter is -13 dBm. A doubler feeds the sub-harmonic mixer on the receive side. The receiver achieves 35 dB NF and dissipates 364 mW. A similar approach was used in [40] to get 400 GHz transmit-receive chipset with -20 dBm of output power.

Coherent systems can provide higher sensitivity compared to direct detection systems, however providing high frequency LO signals remains challenging at these frequencies. Considerable power and silicon area is required to provide high frequency LO signal and to route the LO across the circuits. In this research, various approaches were explored to utilize new circuit design techniques to improve the performance of these types of circuits. Utilizing arrays were found a promising approach to improve the performance of these circuits. Successful implementation of THz signals was demonstrated in CHAPTER 3. In this chapter, the realization of full transmit-receive channels at mmW and sub-mmW frequencies is addressed. New design concepts were introduced to improve the sensitivity of the receivers. Coherent systems were implemented with phase-locked transmit and receive channels. Fully integrated solutions with on-chip PLL and on-chip antennas were implemented to show the possibility of the realization of reasonably high-performance systems utilizing current IC technologies at high mmW and sub-mmW frequencies. The reported circuits in this study show record performance among the reported realizations in silicon technologies.

Due to reduced wavelength, the realization of on-chip antennas is possible, however the limited height of the back-end-of-line (BEOL) of the current IC technologies poses a serious limitation on the performance of antennas. Thus, antennas with GND reflector are very narrowband. In addition, the lossy silicon substrate significantly lowers the gain of the antennas that do not utilize on-chip reflectors. The local-backside-etching technique was utilized to remove the silicon underneath some of the antennas reported in this work to improve antenna gain.

4.2 Fully-Integrated SiGe Transmitter and Receiver with on-chip Antennas

This design deals with the implementation of a fully-integrated 314 GHz transmitter and receiver with high performance, compact size, and low power consumption. High performance on-chip signal sources described in 3.2 was utilized in this architecture to avoid external high frequency sources. The availability of on-chip differential LO source, enables the use of new sub-harmonic switching technique for lower conversion loss and higher sensitivity. In addition, it greatly simplifies the design and layout of the circuit to fulfill the requirement of the array design. Since, the present design will eventually be utilized in larger array system, it is important to minimize the layout area of the circuits to fit in the allocated area within the antenna array.

4.2.1 Circuit design

The current technology features f_T/f_{max} of 300/450 GHz. Thus, considering the insertion loss of the matching network, almost no power gain can be obtained from the transistors above 300 GHz. Alternatively, sub-harmonic circuits and frequency multipliers can be employed. Although fundamental-harmonic direct conversion mixers and detectors

can also be utilized to detect the signals at the receiver side, care must be taken to properly design the circuits for reasonable receiver sensitivity. In this chapter two approaches will be considered for detecting the signals with better sensitivity. Both approaches utilize coherent detection and use LO signal for detecting the incoming RF signals. The first approach utilizes sub-harmonic down-conversion concept which is the subject of the current section. The second approach utilizes fundamental frequency down-conversion with optimized frequency doubler. Both approaches achieve similar performance and excel the existing reported circuits by utilizing novel circuit techniques.

The block diagram of the proposed receiver and transmitter is shown in Figure 60. The transmitter utilizes an active antenna structure where the generated on-chip signal is fed directly into the antenna. The push-push VCO from section 3.2 was modified and utilized as a signal generator at 314 GHz. The receiver utilizes a sub-harmonic configuration with an on-chip, differential, high-power signal source implemented to provide the high frequency LO.

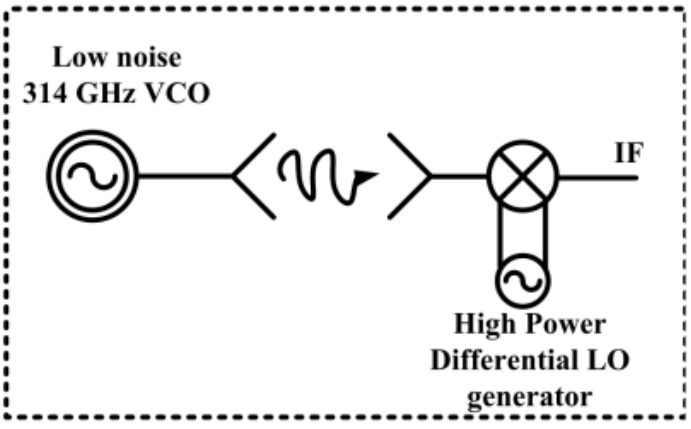

Figure 60. Block diagram of the 314 GHz SiGe transceiver.

Because the active devices cannot provide gain at 314 GHz in this SiGe technology, no LNA is used at the input of the receiver. The system of Figure 60 was chosen in such a way that similar signal sources can be used in both transmitter and receiver. While the second harmonic of a 157 GHz signal generator was utilized in transmitter, a similar signal source can be utilized for sub-harmonic down-conversion at the receiver side. This system architecture was designed to have the capability to phase lock these signal sources together for future implementation. The current system utilizes free running signal sources; however it was modified to fully phase -locked system at 230 GHz which will be described in the next sections.

4.2.1.1 Transmitter

Utilizing a chain of amplifiers and frequency multipliers is the traditional approach to produce RF power at mmW and sub-mmW frequencies from the low frequency signals [29], [102], [26]. Although it can potentially provide higher output power compared to harmonic oscillators, the complexity and high DC power consumption of this approach, as well as stability considerations which come into play from the inter-stage amplifiers, becomes a serious challenge for such complex systems. In addition, the large footprint of the entire circuit, makes it less desirable for array implementations. Harmonic oscillators on the other hand can produce similar power level, with compact form factor which is desirable for array implementation. The main drawback of this approach comes from the narrowband operation specially at mmW frequencies. Nevertheless, by improving the technology, the performance and tuning range of these sources have also been improved. For instance, the implemented PLL presented in CHAPTER 2 provides more than 10% locking range at D-band which is sufficient for most of the applications. Novel circuit

design techniques have also been explored to improve the tuning range of these types of signal sources [32], [78].

Our approach in the present work is to generate the required signal for the transmitter from the second harmonic of a push-push oscillator. Because of the higher f_{max}, a high performance, high power oscillator can be designed to provide reasonably strong second harmonic content with a compact size and small DC power consumption. The circuit uses a modified version of the push-push Colpitts topology presented in section 3.2. The schematic of the modified circuit was reproduced in Figure 61 along with the die micrograph. The etched area of the silicon underneath the antenna is also clear from this picture where the other side of the chip is clear from the transparent Sio_2. Since the push-push node provides virtual GND at fundamental frequency, including the antenna should not affect the operation of the circuit significantly. However, it is important to assure that common mode is not excited. Resistive losses in common nodes, more specifically the common base node are typically utilized in Colpitts VCOs to avoid the common mode excitation. Since the antenna is directly attached to common base node, and assuming the input impedance of the antenna is approximately 50 ohms, the common mode cannot be excited at the oscillation frequency. At lower frequencies, the antenna demonstrates higher impedance, precluding the common mode excitation. However, there is a chance of common mode excitation at higher frequencies where the antenna could demonstrate a small input impedance to the circuit. In the current design, the transistors cannot provide any power gain at those frequencies, however care must be considered when utilizing this topology to investigate the instability possibility across all the frequency ranges where the transistors could provide power gain.

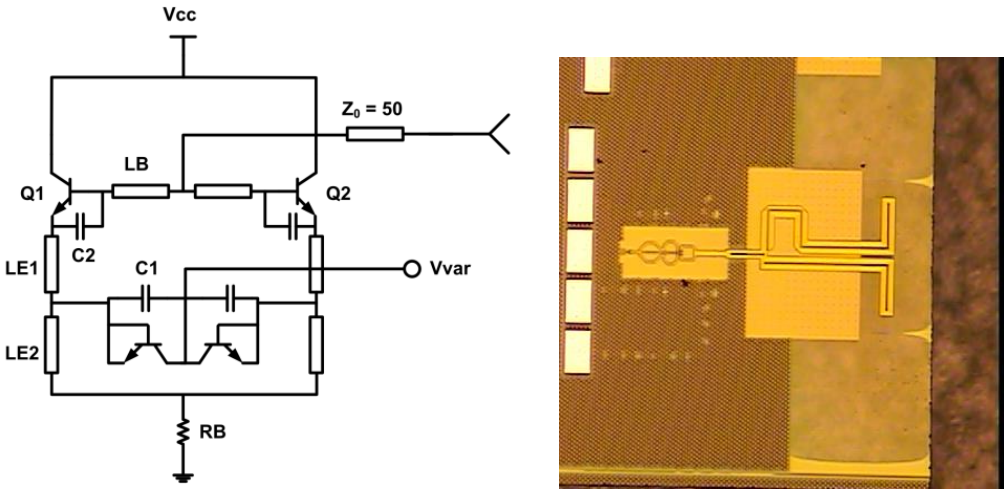

Figure 61. Scematic diagram of the 314 GHz active antenna structure (left), and Die micrograph (right).

The fundamental oscillator operates at 157 GHz and provides a 314 GHz signal at the push-push node. SiGe HBTs with shorted emitter-base junctions were used as the varactor for the circuit, and small MiM capacitors were also employed with the varactors to ensure that the oscillator starts up safely in the case of inaccuracy of SiGe HBT models at these extremely high frequencies. The future implementation of this VCO avoids these MiM capacitors for better tuning range. All the transmission lines, VIA connections and MiM capacitors were carefully EM simulated in order to obtain the most accurate estimation of the operational frequency and the output power. Careful EM simulation becomes even important consideration when considering the narrow bandwidth of the VCO tuning range and antenna bandwidth. The antenna impedance does not significantly affect the operation of the push-push VCO, thus antenna bandwidth does not pose a serious limitation when used in this configuration. In other words, the antennas would still radiate efficiently even in the presence of any possible frequency shift.

4.2.1.2 Antenna

A Yagi-Uda antenna was designed to occupy small space and produce a highly directional radiation pattern. The antenna consists of a driven dipole with a truncated microstrip ground-plane which acts as a pseudo-reflector for the quasi-Yagi antenna. A 180 degrees microstrip balun was utilized in the body of antenna for balanced signal creation for the dipole. Using the localized back-side etching (LBE) technology of ihp Microelectronics, a cavity was etched under the antenna to boost the performance. The LBE was modeled in 3D EM software. Design process of a similar Yagi-Uda antenna which utilizes LBE at D-band frequencies can be found in [112].

4.2.1.3 Receiver

Since the SiGe HBTs cannot provide useful gain at 314 GHz, the receiver front-end does not include an LNA. Instead, the sub-harmonic mixer receives the input RF signal from the antenna and directly downconverts it to IF frequency. In [43], the receiver at 220 GHz employs a three stage LNA utilized at the same technology of the present design. The NF of the receiver was 18 dB. The sub-harmonic passive receiver in the present design achieves a similar performance without additional DC consumption or silicon area.

Designing low noise and low conversion loss sub-harmonic mixer is extremely important for the present receiver. Due to absence of LNA, the sensitivity of the receiver is solely determined by the NF of the down-conversion mixer. In [31],[43] active mixer was employed for the RF down-conversion, with considerably high NF. Since the transistors cannot provide any power gain at those frequencies, utilizing the biased transistors in the mixer, act as noise source right at the input of the receiver and

significantly degrade the NF. Thus, the current design utilizes a passive type of mixer for the down-conversion at the RF input of the receiver. The conversion loss of the passive mixer, determines the NF and sensitivity of the receiver in this case. It is known that these types of passive mixers require high LO power to minimize the conversion loss. The problem is even further challenging when sub-harmonic operation is desired. Balanced LO signals with high power can enable relatively low-loss sub-harmonic down-conversion. Thus, a local on-chip signal source with high output power can significantly help to reduce the challenges associated with differential LO routing and amplification.

The simplified schematic of the proposed passive sub-harmonic switching is shown in Figure 62.

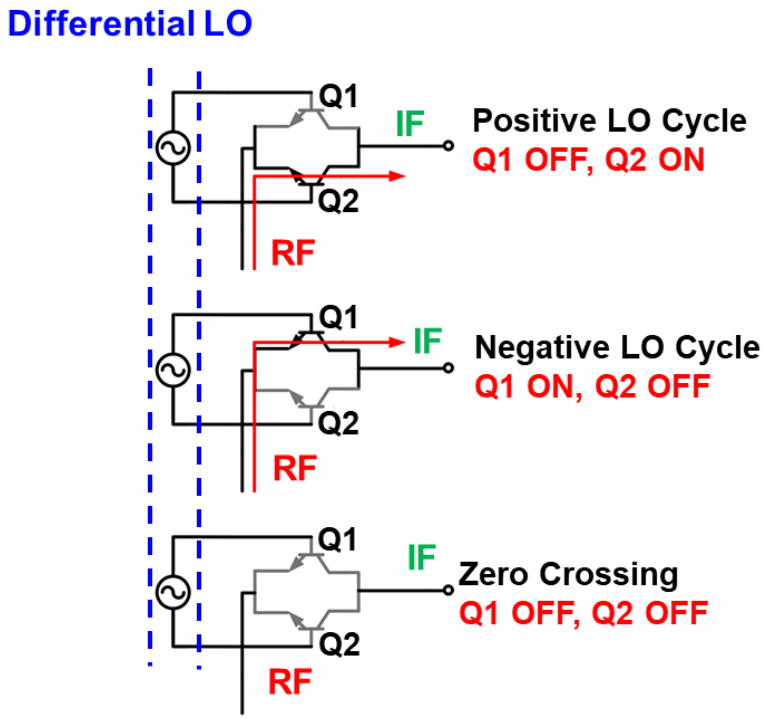

Figure 62. Principal of operation of the proposed sub-harmonic mixer.

The biasing and matching networks are not shown in the figure for simplicity; however, the mixer operates in passive mode with lightly-biased base-emitter junction. When LON is positive and above the turn-on voltage of transistors, Q1 is ON, Q2 is OFF, and Q1 exhibits a small resistance between the collector and emitter terminals thus, passes the RF signal to IF port. When LON becomes negative, LOP becomes positive. Once LOP becomes larger than the turn-on voltage of Q2, Q2 turns ON, while the Q1 is OFF and exhibits the same small resistance between the collector and emitter terminals, with similar path for the RF port to IF port. However, for a small period over the zero crossing of the LO signal, and while the LO signal is below the turn-on voltage of the transistors, both transistors turn OFF and block the RF path to the IF output. Therefore, RF signal could pass to the output IF port a couple of times during each LO cycle and it is stopped from output a couple of times during the LO zero crossings. The phenomenon resembles multiplication of the RF signals to the sequence of one and zeros by the application of LO signal. The frequency of this multiplication is effectively twice the frequency of the LO signal. Thus, the sub-harmonic operation could effectively be accomplished with this architecture. By applying a base-emitter biasing to these transistors, the threshold voltage in which the transistors could conduct increases, and the conduction angle of the transistors reduces. This can change the duty cycle of the resultant modulation and can improve the 2^{nd} harmonic content of the modulation waveform. Conversion-loss depends on the ON-resistance of the SiGe HBTs and the effective modulation by the LO signal. Therefore, there is an optimum bias voltage for the base terminals of SiGe HBTs that produces minimum conversion loss, and this bias voltage is less than the turn-on voltage of the transistors.

The RF port was matched to the antenna through a matching network, and the LO port also was matched to oscillator output to receive the optimum signal power from the oscillator. The IF frequency of 20 GHz was originally selected to make a compact matching network at the IF port; however, since the on-chip LO source was employed, the tuning range was limited, therefore a small shift in the high frequency transmit signal could entirely push the IF signal out of the IF bandwidth and hence possibly reject it. For these reasons, the IF matching was omitted in the present design. Better NF and lower conversion loss can be obtained with IF matching at the output. Quarter-wave stubs have been utilized at the different ports of the mixer to block the port-to-port signal leakage and facilitate matching network design. Since the LO signal is differential, there is a good isolation between the LO port from the RF and IF ports. This facilitates optimizing the LO matching network without considerably affecting the matching of the other ports. In addition, the $\frac{\lambda}{4}$ line at LO frequency appears as a $\frac{\lambda}{2}$ line at RF frequency which is almost twice the LO frequency. Therefore, shorted $\frac{\lambda}{4}$ lines at LO frequency can be placed in LO ports to isolate the LO port from the RF port for independent matching of the RF port without affecting the LO port matching. The complete schematic of the designed sub-harmonic receiver including the designed matching network is shown in Figure 63.

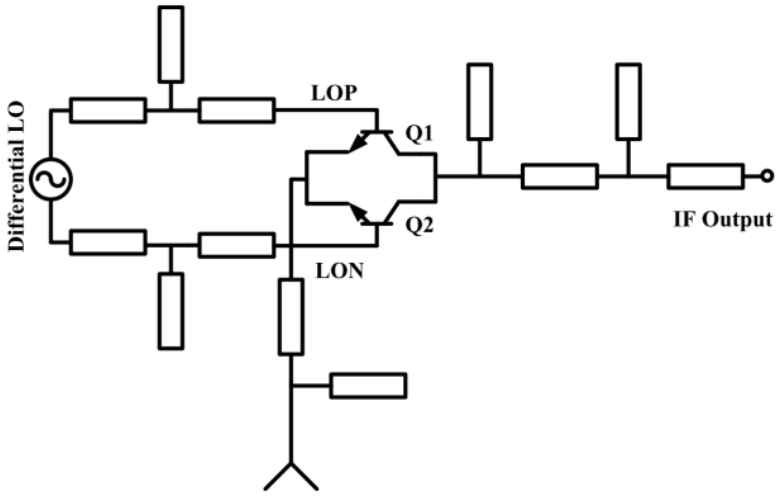

Figure 63. Schematic of the subharmonic receiver at 314 GHz.

The architecture of this circuit has similar operational principal to well-known "asymmetric antiparallel diode pair'' (ASAP) sub-harmonic mixer. However, the present design operates as sub-harmonic resistive mixer with balanced symmetrical operation which automatically rejects the fundamental LO signal. The port to port isolation of the proposed architecture is also superior than ASAP topology.

4.2.2 Measurement Results

A WR2.8 VDi even-harmonic mixer was used to measure the 314 GHz signal. To measure the conversion loss and the gain of antennas, an additional reference circuit was implemented which directly connects the transmitter to the receiver. The transmitter signal source was implemented separately. The conversion loss of the receiver was obtained by measuring the power of the transmitter and the power of the down-converted signal at the output of the reference circuit. Figure 64 shows the block diagram and die photo of these reference circuit.

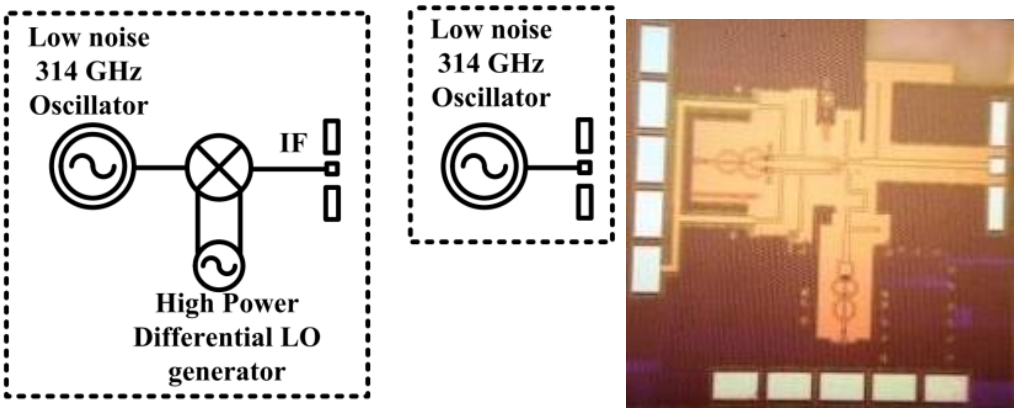

Figure 64. Block diagram of the reference circuit for measuring the conversion gain of the receiver (left). Block diagram of the push-push VCO (middle), and die micrograph of the reference circuit (right).

Since the output power of the 314 GHz signal was measured with a 50 ohms instrument, and the input impedance of the receiver was also matched to 50 ohms, the test circuit should provide pretty accurate results. The RF matching network of the receiver was designed assuming small signal behavior; however, the generated power from the 314 GHz VCO in the reference circuit is not small signal and could potentially cause inaccuracies. Simulations show that 1.0 dB additional conversion loss occurs in the reference circuit because of the mismatch caused with relatively large input signal. We note, however, that the output power of VCO in the reference circuit can be reduced by decreasing the bias current to better resemble small- signal conditions. This would enable more accurate characterization.

This additional loss was captured using simulations and the measured conversion gain with the correction is illustrated in Figure 65. This figure also shows the simulated NF of the receiver.

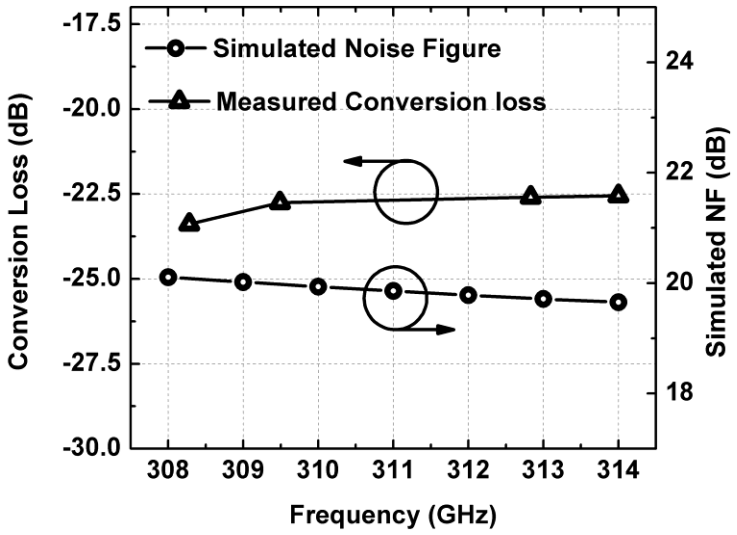

Figure 65. Measured conversion loss and simulated noise figure of the receiver.

To demonstrate the operation of this high frequency link, the transmitter and receiver circuits were placed apart at 5.5 mm, with the antennas facing each other. The received signal was amplified and captured using a spectrum analyzer. Figure 66 shows the measurement setup. To align the antennas, the microscope was first focused on the antenna of the transmitter. The antenna of the receiver was observed afterwards with the same microscope and the same focus conditions. The z dimension of the chuck was then adjusted with micromanipulator such that the antenna of the receiver also remains in the focus point of the microscope. This technique ensures the perfect alignment between the antennas.

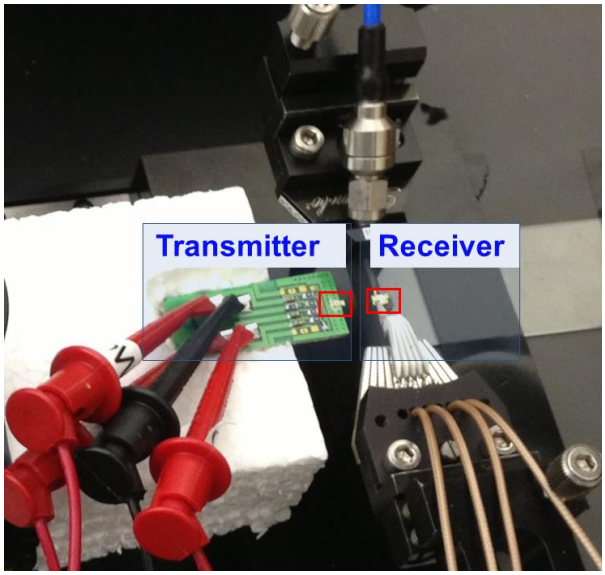

Figure 66. Measurement setup of the 314 GHz transmit-receive link.

Figure 67 shows that the received signal is very close to the designed IF frequency of 20 GHz. Also shown is the down-converted signal from the reference circuit. Antenna gain can be approximately calculated by assuming the free space path-loss and subtracting the power of the received signal from the signal power at the output of the reference circuit.

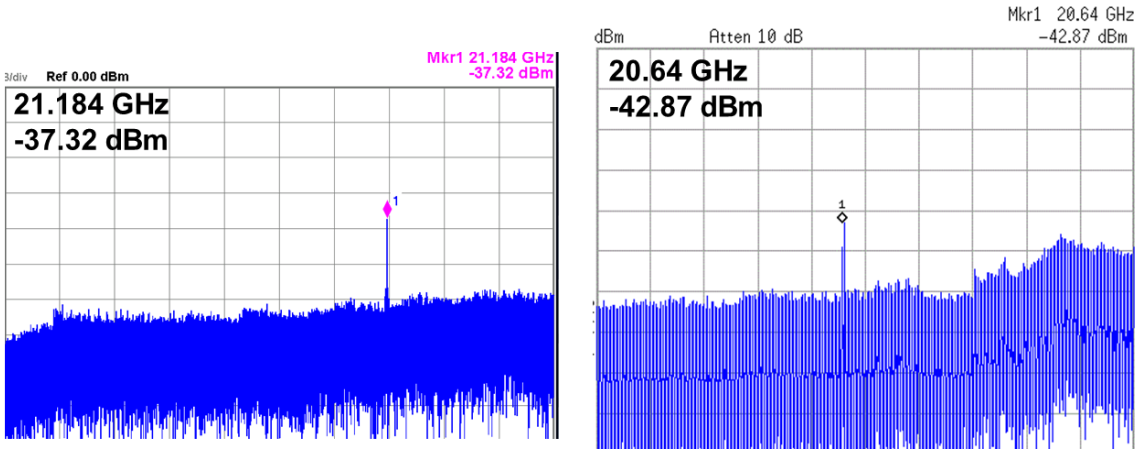

Figure 67. The detected signal from reference circuit without de-embedding (left), and the detected signal at the output of the receiver after amplification (right). The distance between the transmitter and receiver is 5.5 mm.

The results of this work are compared with the published silicon based state-of-the-art in Table 5.

Table 5 Measurement summary and comparison with the state-of-the-art.

Ref	Freq (GHz)	NF (dB)	Gain (dB)	Output Power (dBm)	DC Power (mW)	Technology
[43]	321	36/32	-10	-	3000	130nm SiGe
[31]	374	35	-7	-13 (EIRP)	364	130nm SiGe
[40]	412	-	-34	-20	118	130nm SiGe
This work	**314**	**19.5 (simulated)**	**-22.5**	**-8**	**132**	**130nm SiGe**

4.3 230 GHz Locked Transmit-Receive Module with on-die Antenna

The utilized signal sources in the transmit-receive chipsets of 314 GHz system presented in previous section, were not synchronized to each other, and were not locked to an externally predefined reference signal. Those free running sources were still, stable enough to considerably reduce the IF bandwidth for lower noise and reasonably high-resolution imaging applications. However, for communication and ranging applications, it is necessary to control the frequency of the signal precisely. In addition, for imaging applications, since only a single tone signal is required, the IF bandwidth can be decreased

considerably for significantly better performance in coherent systems with phase locked signal tone.

In conventional RF systems, an external LO is used or a central PLL generates the LO signal and this signal is routed across the entire chip for transmit and receive channels. Where extra drivers and amplifiers are utilized in the LO distribution network. However, LO distribution is challenging at mmW and sub-mmW frequencies and consumes significant amount of DC power. Routing differential and multiphase signals is even further challenging. An alternative solution to this problem is to utilize local signal sources and first presented in the current research [12]. However, locking the phase of these sources can be challenging. Th methodology proposed in section 3.3 provides a robust way to perform strong phase locking between the signal sources. In the present work and following that methodology, signal sources of the transmitter and receiver channels in the present design, were phase locked to each other and to an external well-defined crystal oscillator using an on-chip PLL. In addition, considering the capabilities of the utilized technology, a less aggressive operational frequency was chosen for this study, where the NF_{min} of the transistors are lower compared to 314 GHz, and transistors can possibly provide small power gain if needed. This improves the receiver sensitivity and provides more output power at the transmitter. The proposed technique with synchronized local signal sources, has advantages compared to traditional approach. A similar or less DC consumption which was utilized in drivers and amplifiers of the LO distribution network, was used in local oscillators in the new design. However, the proposed technique features a better phase noise performance because of the coupled VCO network. In addition, the availability of

high power and local balanced signals from the VCOs, mitigates the complexity of amplifier and Balun design.

The system architecture of the fully integrated transmit-receive (TR) channel is shown in Figure 68. The details of the circuits and PLL is omitted in this figure for simplicity. Because of the high insertion loss and low isolation of the front-end switch at 230 GHz, and considering the reasonably small form factor of the on-chip antennas at 230 GHz, the present TR utilizes two separate on-chip antennas for transmit and receive channels and avoids the front-end duplexer switch.

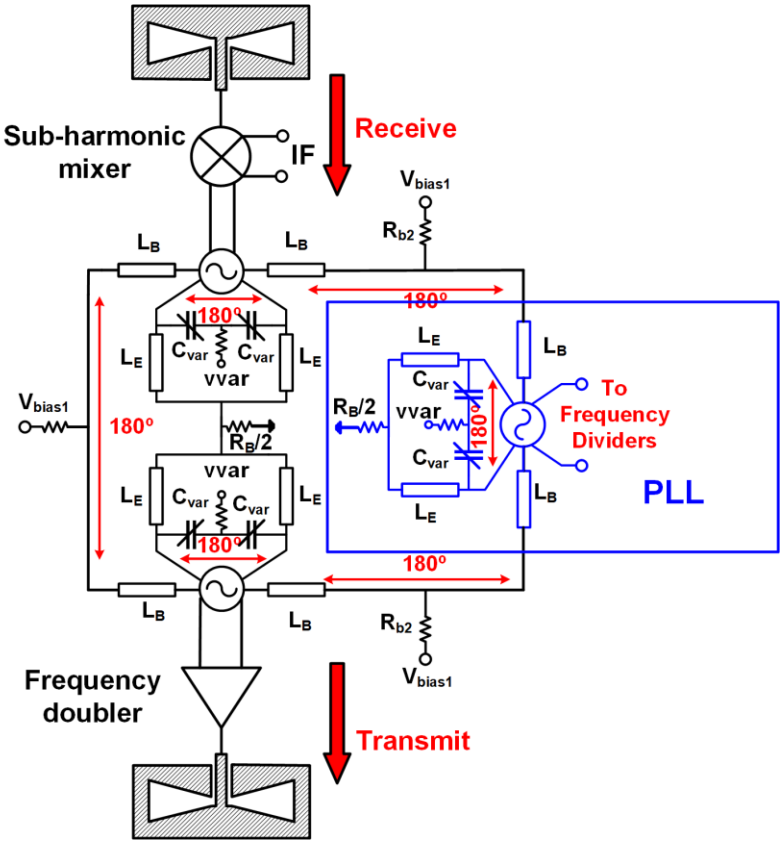

Figure 68. Block diagram of the fully integrated 230 GHz transmit-receive channel.

The receiver utilizes the same sub-harmonic mixer topology of Figure 63 which is redesigned at 230 GHz. The transmitter utilizes similar VCO-multiplier combo circuit to generates high power signals at 230 GHz. Both the transmit and receive channels utilize separate high performance local oscillator circuits. These oscillators are locked together and to an extra interface oscillator which drives the frequency dividers of the PLL loop.

Figure 69 shows the simulated conversion gain and Figure 70 shows the simulated noise figure of the receiver subharmonic mixer. All the components within the system in Figure 68 are matched to each other at 230 GHz for better power transfer and lower NF using large signal harmonic balance simulations.

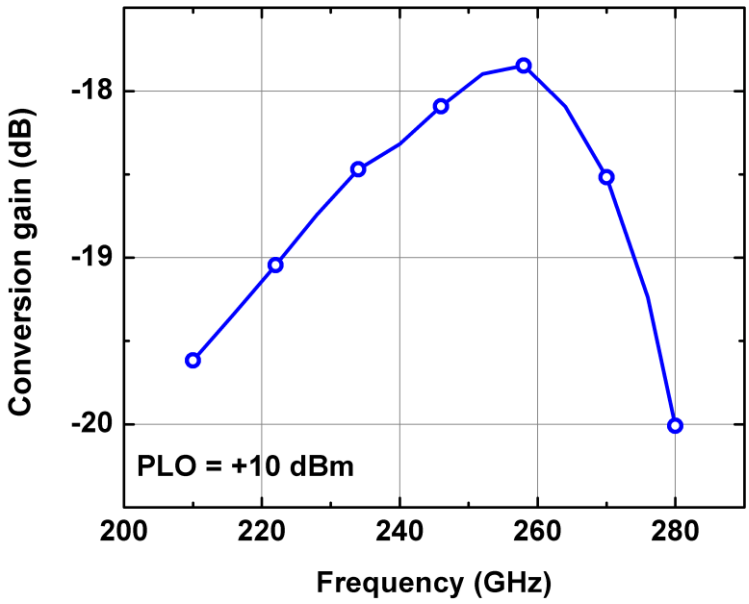

Figure 69. Simulated conversion-gain of the sub-harmonic receiver.

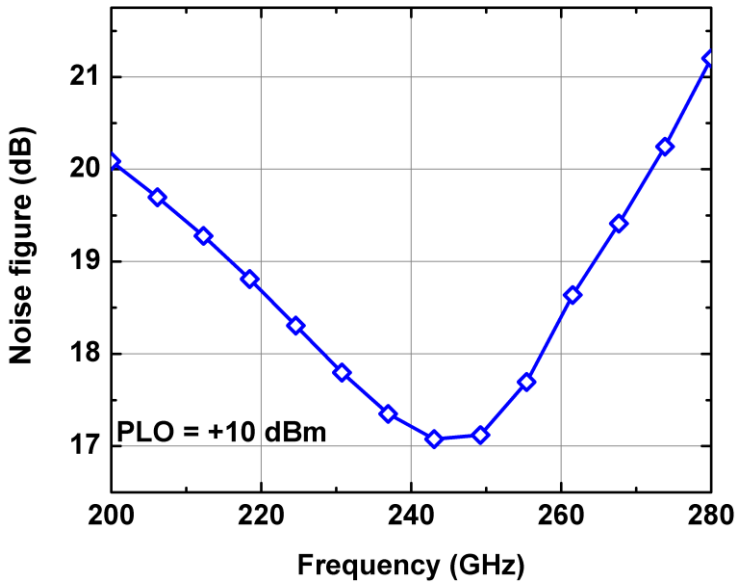

Figure 70. Simulated noise figure of the sub-harmonic receiver.

As explained in section 4.2, there is an optimum biasing point for the SiGe HBT transistors of the sub-harmonic mixer which minimize the NF and conversion loss. Figure 71 shows the simulated results of the NF a of the receiver sub-harmonic mixer with respect to the biasing of transistors. Biasing the transistors becomes even more important when LO power is not adequate to completely switch the transistors. Simulations show that NF and gain have small dependence to the biasing of the base-emitter junction when the LO power is high and could completely switch the tarnsistors. The circuit was implemented in ihp's 130 nm SiGe technology. Figure 72 shows the die micrograph of the circuit. Additional circuit with probing pads instead of the on-chip antennas were also implemented for characterization purposes which is shown in the same figure.

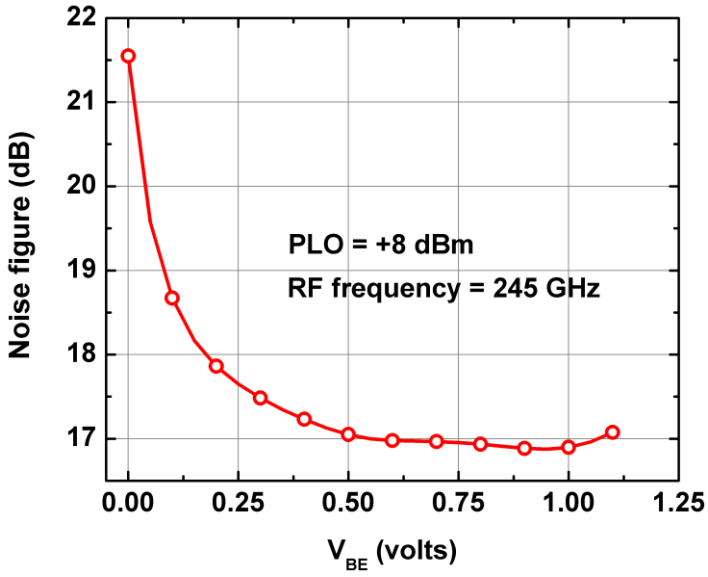

Figure 71. Simulated noise figure of the sub-harmonic receiver with respect to base-emitter biasing. RF frequency was 245 GHz.

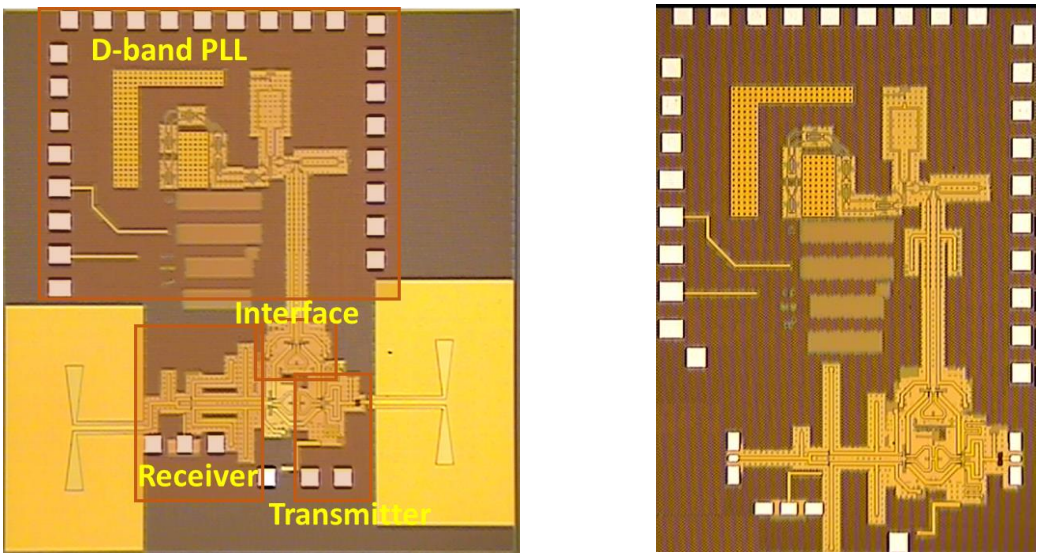

Figure 72. Die micrograph of the 230 GHz fully integrated T/R module.

4.4 230 GHz T/R Module with Fundamental Direct Conversion Mixer

Because of the availability of high power source at 230 GHz by utilizing the proposed VCO-multiplier combo circuit, a direct conversion with fundamental signal at 230 GHz can also be considered as an alternative topology to perform low conversion loss direct conversion detection. To complete this study, a fundamental direct conversion receiver was designed at 230 GHz. This study enables a comparison between two architectures. One approach utilizes sub-harmonic detection with strong high-power differential source at half the RF frequency. The other approach utilizes fundamental down-conversion at RF frequency with a frequency multiplied LO signal which is generated from the same differential source as the other architecture. A full T/R module was implemented in the same technology platform with similar components as the T/R module from previous section. The block diagram of the new T/R module is shown in Figure 73. The schematic diagram of the fundamental frequency down-conversion mixer is shown in Figure 74. The architecture of the mixer is single-side-band (SSB), where Q2 serves as the switching mixer. Q1 receives the RF signal, and provides some isolation between the RF and LO. The Q1 transistor was lightly biased with 160uA current to minimize the conversion loss without degrading the NF. As mentioned earlier, since the transistors provide small power gain at these frequencies in perfect matching conditions, further biasing the transistors degrade the NF without considerable improvement in conversion-gain. Base-emitter voltage of Q2 can accurately be controlled with additional biasing knob from the LO port. This flexibility provides a means to control the conduction angle of the Q2 for minimum conversion loss, as explained in previous section.

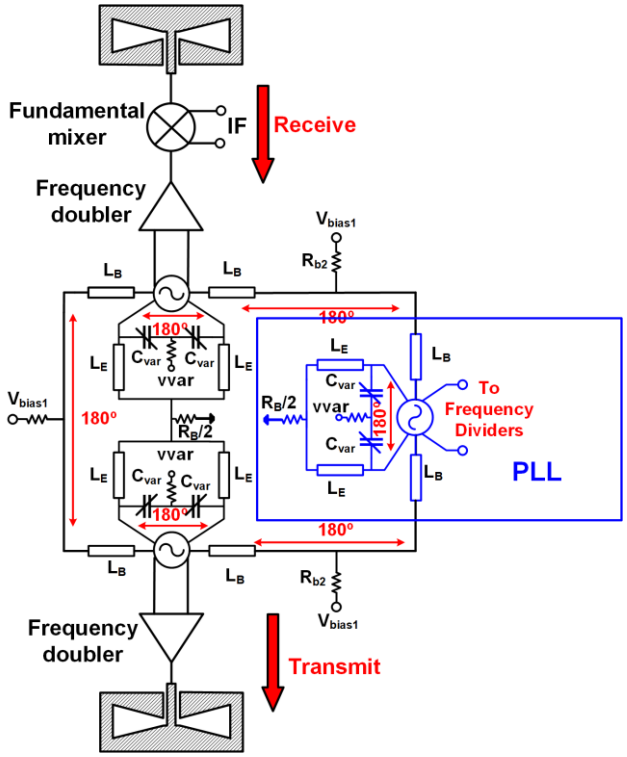

Figure 73. Block diagram of the fully integrated 230 GHz transmit-receive channel with fundamental frequency down-converter.

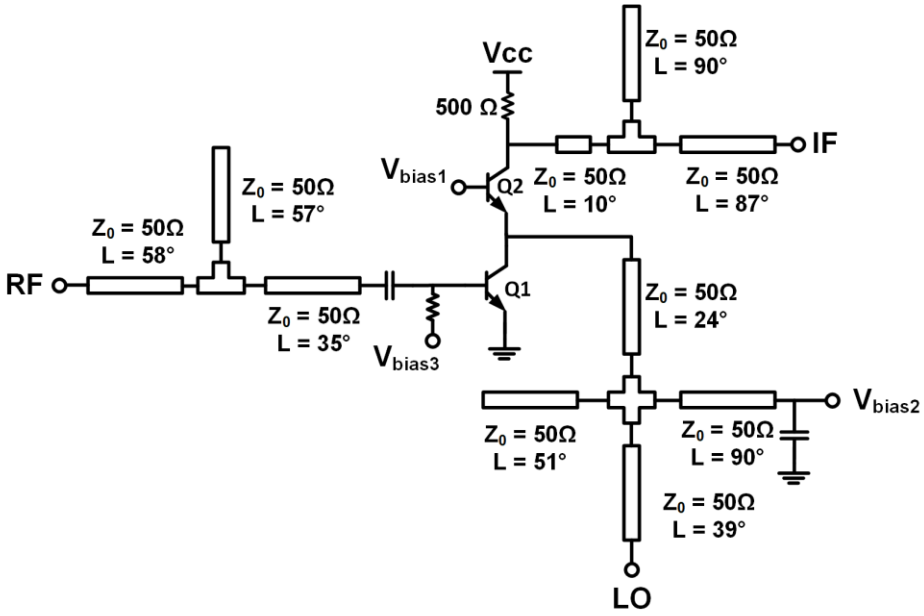

Figure 74. Schematic diagram of the fundamental frequency down-conversion mixer at 230 GHz.

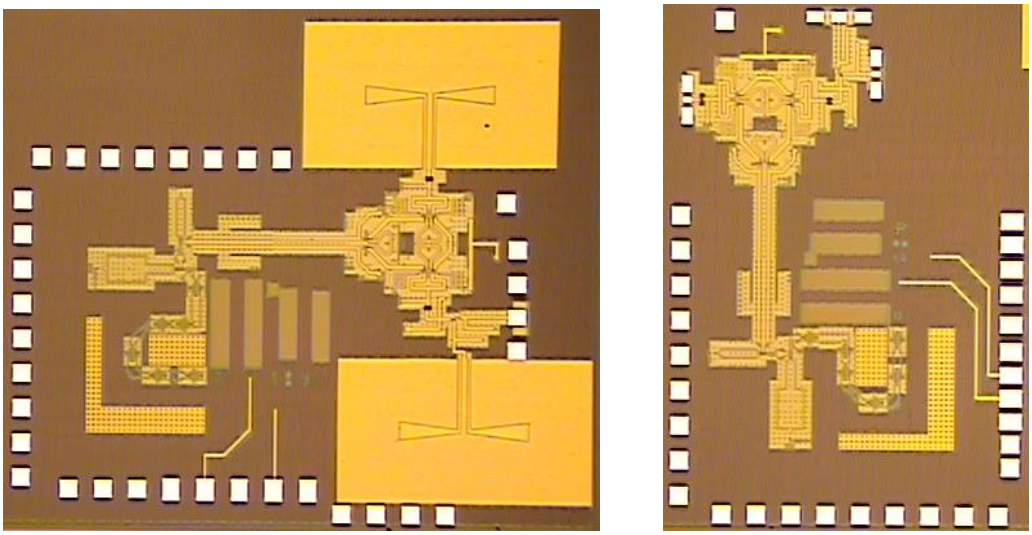

Figure 75. Die micrograph of the 230 GHz T/R module with fundamental direct conversion receiver. The full T/R with antennas (left), and T/R with output pads instead of antennas (right).

Figure 75 shows the die micrographs of the implemented circuit including the circuit with on-chip antennas and the same circuit with probing pads instead of antennas for further characterization.

Figure 76 shows the simulated conversion gain of the fundamental frequency down-conversion receiver and compares the result with the conversion gain of the sub-harmonic passive receiver presented in previous section. The switching transistor of the fundamental frequency mixer was biased at 160 µA for this simulation. Thus, significantly better conversion-loss was achieved compared to fully passive sub-harmonic mixer described in previous section. Further increasing the biasing current, degrades the receiver NF without noticeable improvement in the conversion gain. In fact, the NF is better metric to compare the sensitivity of the receivers, since conversion gain can always be provided at IF frequency at almost no cost.

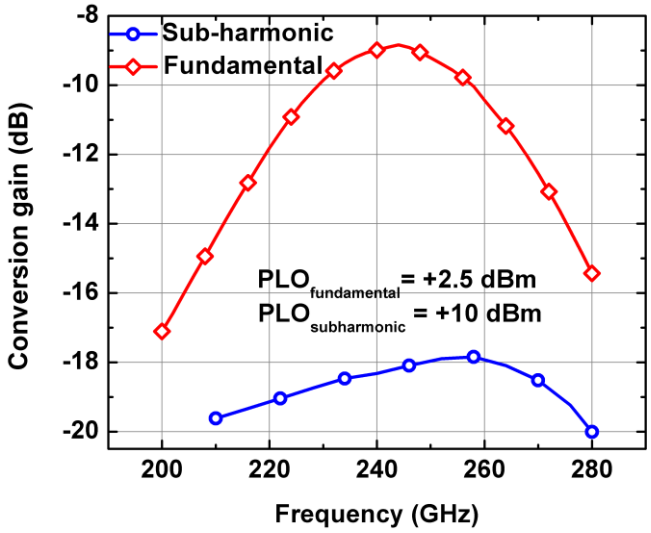

Figure 76. Simulated conversion gain of the fundamental frequency receiver, compared to the sub-harmonic receiver.

Figure 77 shows the simulated NF performance of the receiver front-end and compares the result with sub-harmonic down-conversion receiver. Comparable performance can be achieved utilizing either technique. The LO power is an important parameter in both receivers.

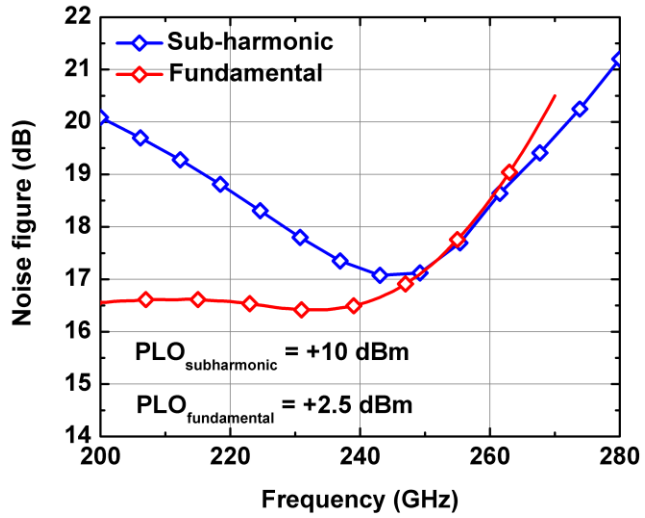

Figure 77. Simulated NF of the fundamental frequency receiver compared to sub-harmonic receiver.

4.5 Fully Integrated D-band Transceiver

The transceivers presented in the previous sections utilized SiGe HBTs at beyond the frequencies where the devices could provide power gain. A transistor without the power gain can only be utilized as switch. Therefore, the receiver front-ends in the previous sections were used innovative passive types of structures for frequency down-conversion. It is expected that silicon devices could march the path toward the f_{max} of 1 THz within the upcoming decade [18]. With those types of devices, sub-mmw circuits with better performance can be designed for higher sensitivity and higher RF power. Nevertheless, arrays can be utilized to obtain better performance. In this section, the design of a T/R module at 120 GHz is presented to study the possibility of fully integrated T/R modules in silicon and at frequencies beyond 100 GHz. The SiGe HBT transistors can provide sufficient power gain with low NF at this frequency range. The module is fully integrated with on-chip PLL and on-chip antenna. In addition, a front-end switch was also designed which provides reasonably low insertion loss with reasonable isolation to enable a single antenna for both transmit and receive channels.

Figure 78 shows the block diagram of the D-band T/R module. The fundamental frequency PLL from CHAPTER 2 was used in this design. Since the PLL could provide high power at D-band frequencies, it can be utilized in transmit channel without a need for additional power amplifier. Thus, one of the differential outputs of the PLL was directly routed to the output, while the other output was utilized as an LO source in down-conversion mixer. A similar coupled VCO approach was utilized in the body of the PLL to separate the output RF power from the PLL feedback loop for higher output power.

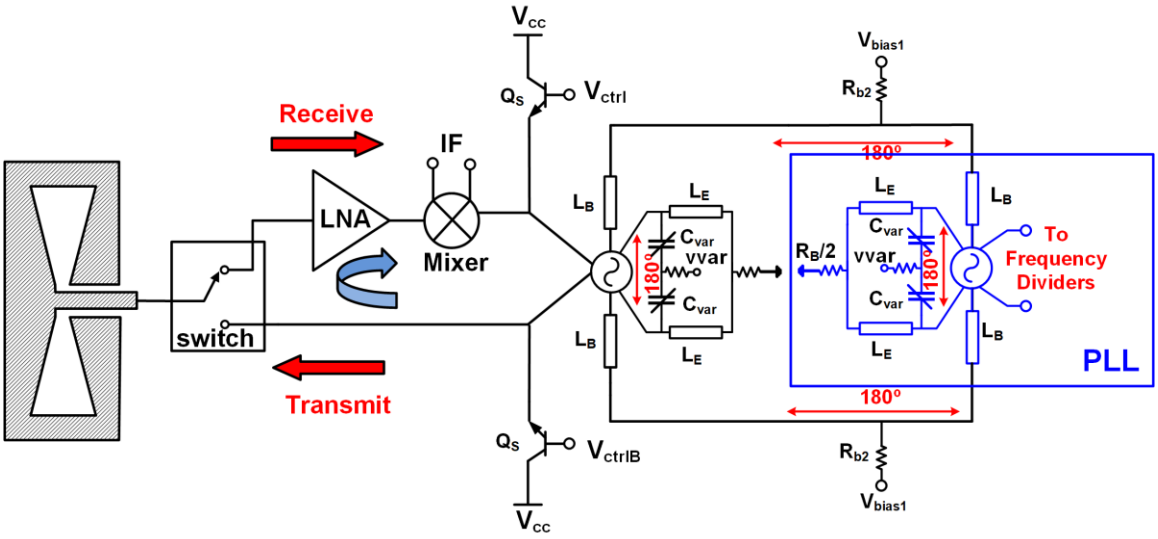

Figure 78. Block diagram of the fully integrated D-band TRX.

Because of the availability of 120 GHz fundamental phase-locked source, a direct conversion receiver topology was selected for the present design. The front-end switch and LNA from [113], [114] were redesigned at 120 GHz with improved performance. The switch isolation is still not adequate for full-duplex operation of the T/R channel. The LO leakage to LNA input is still strong enough which can saturate the receiver. Thus, extra switching mechanism was designed to bypass the strong transmit signal from the receive channel during the receive time to avoid receiver saturation. These switches are shown in Figure 78 (Q_S transistors). These switches are turning ON and OFF alternatively by the application of V_{ctrl} and complementary signal V_{ctrlB}. These devices were designed for short switching time such that it can turn ON rapidly before the reflection signal comes back from the target for the envisioned radar application.

Because of the high LO frequency, the LO to IF leakage is sufficiently attenuated at IF port and LO to IF leakage was not concern in this design. Therefore, an SSB mixer was chosen which can operate with single-ended LO from the PLL. Figure 79 shows the

schematic of the designed down-conversion mixer. The topology is similar to the one utilized in section 4.4, except than the LO feed port. The mixer is biased in the present design to minimize the conversion loss. The LO port was carefully matched to mixer for sufficient power transfer from the PLL. Although there was a long distance between the PLL output and the mixer, the LO driver was omitted because of the high output power of the PLL, to save DC power and for simplicity of the layout. An IF frequency of 1 GHz instead of DC was considered for this design to avoid the possibility of self-mixing within the mixer because of LO to RF leakage. An extra biasing knob was designed at emitter of the Q2 SiGe HBT to control the conduction angle of the Q2 switching device.

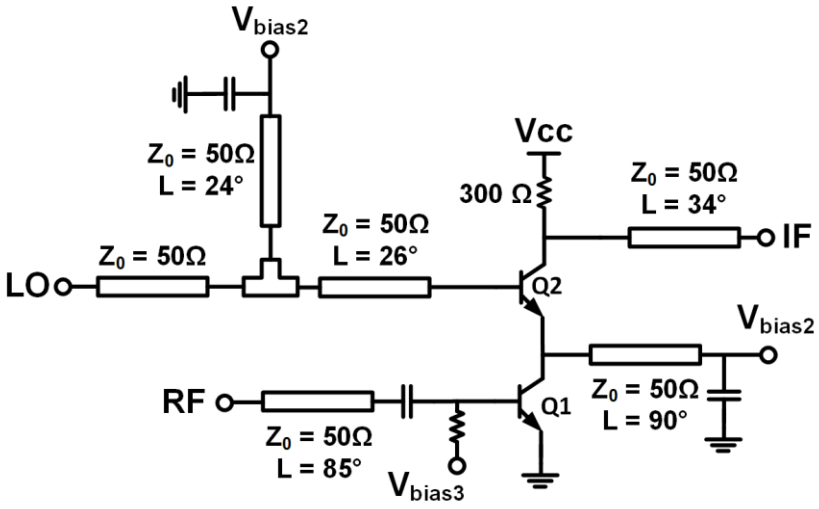

Figure 79. Schematic diagram of the D-band fundamental frequency down-conversion mixer.

Figure 80 shows the die micrograph of the implemented circuit. The circuit measures 2.5×2.2 mm^2 including the on-chip antenna.

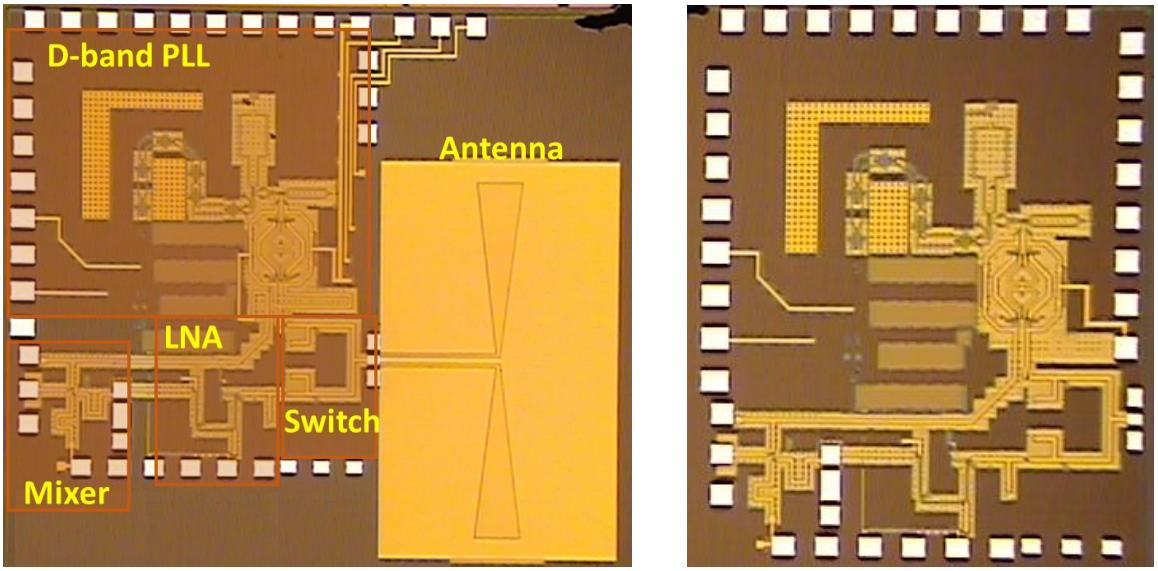

Figure 80. Die photo of the full D-band TRX (left). D-band TRX with probing pads instead of antenna (right).

Figure 81 shows the simulated input return loss and power gain of the combination of switch and LNA circuits and Figure 82 shows the simulated noise figure of the receiver. Observe that designed NF is very close to minimum possible NF from the system. This is the result of simultaneous noise and power matching technique utilized in this design. The optimum noise impedance was brought to the location of the optimum power transfer impedance at the input by proper design of the transistor size and biasing current.

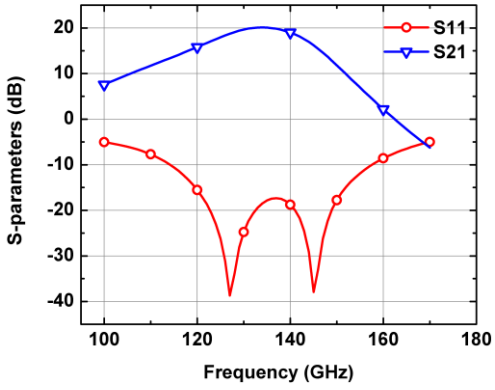

Figure 81. Simulated S-parameters of the LNA and switch combination.

Figure 83 shows the simulated conversion gain of the entire receiver. The interstate matching between the LNA and mixer was deliberately shifted in frequency to obtain the behavior of the staggered LNA and to increase the bandwidth. The peak conversion gain of the LNA and mixer in this technique were separated apart in frequency by proper design of the matching networks.

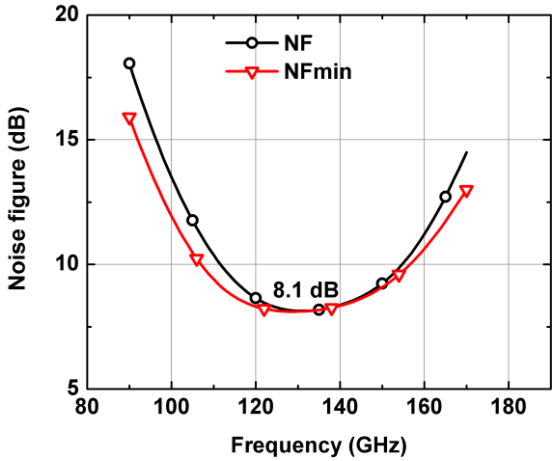

Figure 82. Simulated noise figure of the receiver compared to minimum possible noise figure.

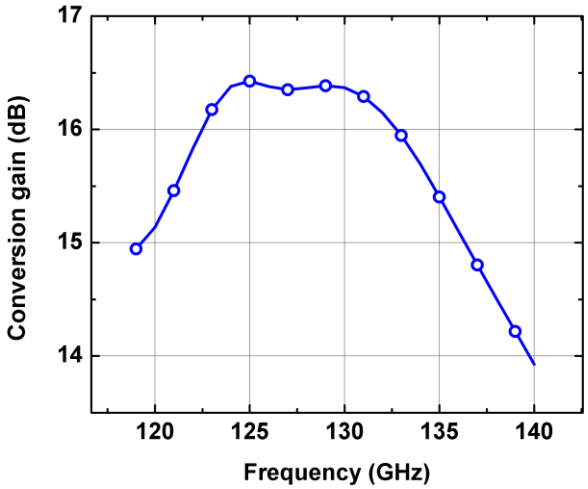

Figure 83. Simulated conversion gain of the entire receiver.

CHAPTER 5. INVESTIGATION OF THE OPERATION OF RF CIRCUITS UNDER EXTREME ENVIRONMENT CONDITIONS

5.1 Introduction

The common definition of extreme environments includes the operation under harsh environmental conditions such as operation under high pressure, chemical corrosion, extreme temperatures and radiation intensive environments. The study in this research however, focuses on the extreme environment present in space which particularly includes the operation under wide temperature variations down to cryogenic temperatures as well as radiation intensive environments. Before the current research, no study was existed on the effect of single-event transients (SET) on high frequency and mmW circuits. The findings in the current study enables understanding of the SET effects on RF and mmW circuit and systems. Several experiments were conducted and supported with analysis and device, and circuit level simulations. The proposed modeling methodology in the present research agrees closely with experimental data and offers a fast and accurate way to simulate the SET on RF systems. In addition, the novel methodology was presented in this research which enables radiation experiments on high frequency circuits by implementing laboratory equipment inside the same chip that contains the circuits under test.

5.2 Cryogenic Operation of Low-Noise Amplifiers

5.2.1 Introduction

Deep space missions require electronic systems that can operate across wide-temperature variations down to cryogenic temperatures. Traditionally temperature control units are being used in satellites to maintain a constant temperature for proper operation of electronic systems. Besides the extra cost, these systems occupy a considerable volume and add considerably to the weight of the system. This is particularly important for CubeSat technologies where there are limitations in the size and weight of the components. Electronic components that can tolerate wide range of temperatures without the need for warm boxes or temperature control units can minimize the size, weight, and power (SWaP) of these systems. In this section, the behavior of a wideband LNA was studied across the temperature as a test circuit to study the operation of receiver components across the temperature.

Wideband communication and radar systems are extensively used in space systems. Wideband LNAs with low noise performance are essential components for these types of systems. However, achieving wideband performance is very challenging and often necessitates a tradeoff between noise performance, power consumption and die area. A few techniques have been introduced in the literature to achieve broadband performance. In [115], a distributed amplifier was utilized to achieve wide bandwidth for UWB applications. The main drawbacks of this technique are related to large silicon area and *dc* power consumption. A common base/gate topology is another technique used to achieve wide band operation; however, the achievable NF using this technique is typically higher.

In addition, since the transconductance (g_m) of the transistor has been set to provide 50 Ω input matching, it cannot be increased for NF improvement. Finally, a feedback technique can be utilized to widen the operational bandwidth. The resistive feedback topology, in particular, is an attractive topology to achieve a broadband operation with small silicon area [116]–[118]. However, in this case the noise coming from the feedback resistor can deteriorate the overall NF. A detailed analysis of the noise performance of an amplifier in the presence of feedback network can be found in [119]. For broadband performance, the value of this feedback resistor needs to be small, which can contribute more noise to the circuit. As an alternative, the g_m of the amplifier can be increased instead of lowering the value of the feedback resistor, to utilize the Miller effect on the feedback resistor. Nonetheless, with advances in silicon technology, it is possible to achieve higher gain-bandwidth product using this approach. In addition, due to the presence of negative feedback, it is expected that this topology could provide more tolerance to temperature variations.

In this study, a wideband resistive-feedback SiGe LNA was designed, and the operation of the LNA was studied across the temperature. It is shown that this LNA can operate in a wide-temperature range, with improved performance at lower temperatures. The LNA achieves the best NF-FoM performance among the other reported wide-band LNAs in silicon technologies.

5.2.2 Circuit Design and Discussion

Figure 84 shows the schematic of the designed LNA as well as the die micrograph of the fabricated chip. The amplifier consists of two stages, with resistive feedback in each stage. The inductor L_B at the base of the first stage was utilized to increase the bandwidth through the inductive peaking effect. This inductor has a small value of 130 pH, and was realized using a transmission line. Feedback and load resistors were utilized using BEOL metal resistors available in this process technology. Since these resistors have considerable physical dimension (63µm length and 5.9µm width), they have both capacitive and inductive parasitics. Although the parasitic inductance does not have major impact at this frequency band, it can possibly affect the out-of-band stability. To model the parasitics of the resistors accurately, these resistors were also EM simulated using Sonnet.

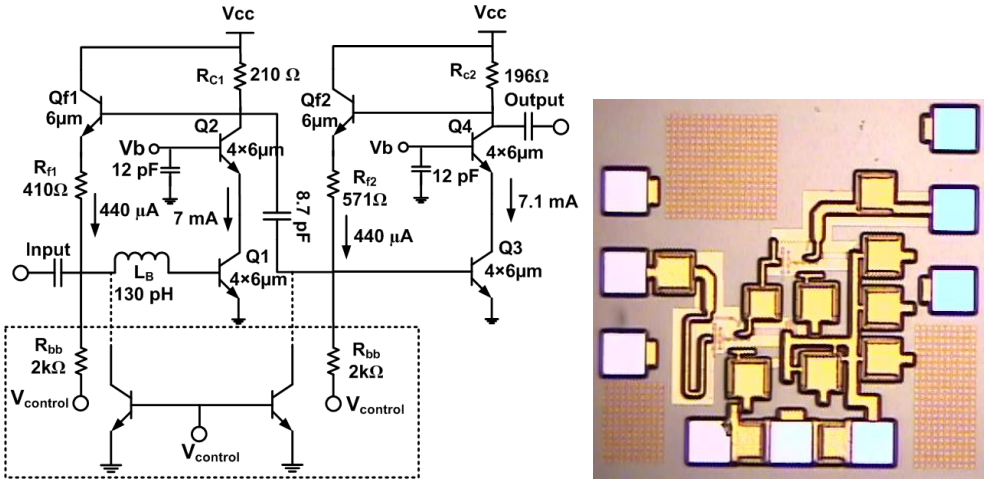

Figure 84. Schematic diagram of the wideband SiGe LNA (left), and die micrograph (right).

The amplifier is self-biased through the feedback loop. This can potentially help the thermal stability of the amplifier across temperature. A SiGe HBT in the feedback loop provides the required dc level shift for proper biasing. The large-value R_{bb} resistors were

realized using polysilicon resistors. These resistors set the feedback current and consequently the biasing current of each amplifier stage. In addition, these resistors have near zero temperature coefficient. The technique that we propose for gain control applies a control voltage to set the biasing currents without breaking the feedback loop. One can use current sources instead of R_{bb} resistors for this purpose. (see Figure 84).

Equation 17 shows the dependence of the biasing current to feedback current I_f.

$$I_c = \frac{-R_f}{R_c} \times I_f + \left(\frac{V_{cc}}{R_c} - \frac{V_{BE}}{R_c} - \frac{V_{BEf}}{R_c}\right) \qquad (17)$$

It is worth mentioning that the complete gain-control unit requires more complicated circuits, which is not in the scope of the current work.

5.2.3 Measurement Results and Discussion

The LNA has been implemented in a 130-nm, 280-GHz f_{max} SiGe platform (GlobalFoundries-8HP). The measured S-parameters of the LNA are compared with simulation in Figure 85. The LNA achieves 14.7 GHz of 3-dB bandwidth with maximum gain of 37.3 dB and more than 42 dB reverse isolation. There is an excellent agreement with simulations, which is the result of accurate modeling, parasitic extraction and EM simulations.

Due to the presence of the negative feedback, it is expected that this amplifier has less sensitivity to temperature variations. To study the sensitivity of the LNA to temperature variations as well as the potential performance improvement at lower temperatures, the LNA was cooled down to 78 K (liquid nitrogen was used in conjunction with a custom-designed ac-cryogenic probe system with accurate temperature control).

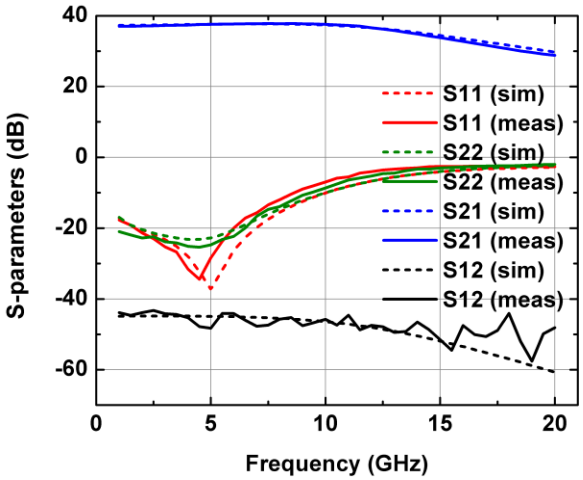

Figure 85. Measured S-parameters compared with simulations.

It is well-known that the performance of a SiGe HBT is improved with cooling [48]. In [120], the performance of a narrowband inductively-degenerated LNA was reported at 15 K. In the present work, we will show that the performance of the resistive feedback LNA is robust to temperature variations. Different circuit components have different thermal properties, each of which can affect the performance of the LNA.

a. Metal resistors (R_f and R_c) have negative thermal coefficients. The value of these resistors increases at lower temperatures, resulting in bandwidth degradation.

b. Built-in potential of SiGe HBTs increase by decreasing the temperature. Thus, decreasing the temperature, results in bias current reduction and gain degradation (see Equation 17.).

c. f_T/f_{max} of SiGe HBTs as well as transconductance (g_m) increase at

lower temperature which improves the bandwidth and gain.

Although mechanisms “a” and “b” can result in gain and BW reduction, mechanism “c” can compensate for this and can even enhance the gain and bandwidth of the LNA. These counteracting mechanisms can effectively reduce the temperature sensitivities of the LNA across a wide temperature range. In addition, the presence of negative feedback helps to further reduce the thermal sensitivities.

Figure 86 shows the simulation results of the effect of different circuit components on the low temperature behavior of the LNA based on the above-mentioned mechanisms. τ_{EC} is the emitter-collector transit time.

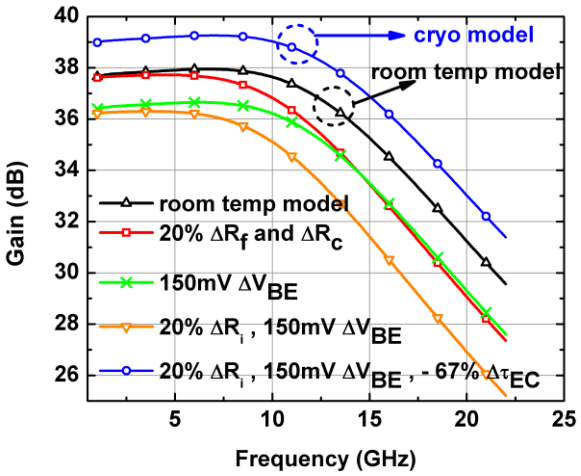

Figure 86. Simulation results showing the effects of various components on the low temperature behavior of the LNA.

R_{bb} resistors were realized using polysilicon resistors which have very small temperature coefficients, and hence near-constant performance across temperature.

Considering these temperature dependencies, there was some initial concern over performance degradation or even instability at lower temperatures. Figure 87 and Figure

88 show the measured results of the LNA at low temperatures. As we can see from these figures, the LNA is stable, while the bandwidth and gain is negligibly affected by lowering the temperature; however, the NF of the LNA was considerably improved, achieving a record average value of 1.0 dB over a 15 GHz bandwidth, with a minimum value of 0.74 dB at 1.0 GHz and 1.49 THz gain- bandwidth product. In addition, one can see that gain and bandwidth of the LNA first begins to degrade by lowering the temperature to 228 K and 178 K; however, the enhanced performance of the SiGe HBT at lower temperatures compensates for the performance loss when further lowering the temperature to 128 K and eventually enhances the gain and bandwidth at 78 K, as indicated in the figure and explained above.

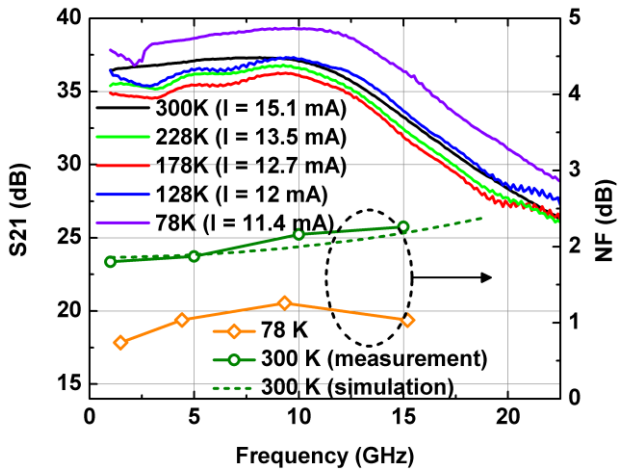

Figure 87. Measured S-parameters and NF at various temperatures.

Figure 88 shows that the LNA maintains its input and output matching across a wide temperature range. Accurate calibrations were performed in these measurements, with repeatable data across the various temperature points.

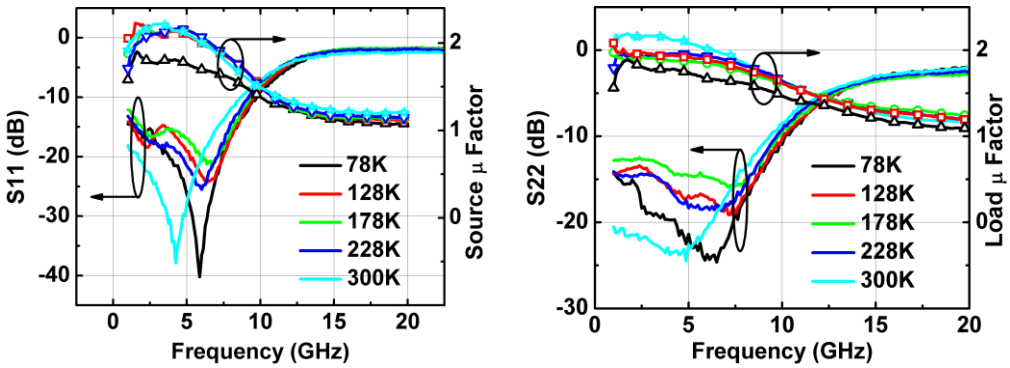

Figure 88. Measured S-parameters and stability factors across temperature. (solid lines: S-parameters, line and symbols: stability factors)

In order to control the gain variation across temperature, the gain control mechanism was implemented in this design to enable flexibility in tuning the LNA's performance.

Figure 89 shows the measured gain at various feedback currents. The simulation results with current sources instead of the R_{bb} resistors are also included in this figure. (see Figure 84). As can be seen from these figures, the gain can be controlled over a 15-dB range without considerably sacrificing the bandwidth and power matching of the amplifier.

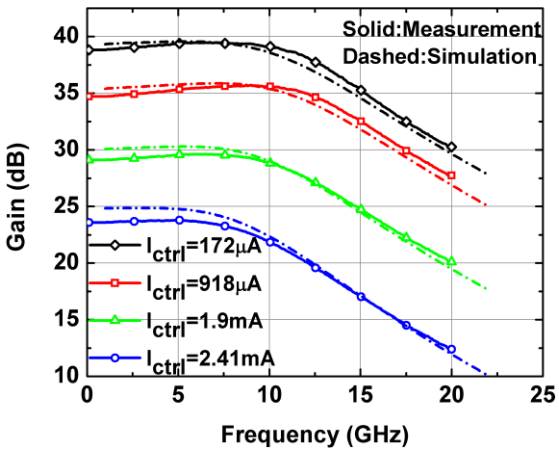

Figure 89. Measured and simulated gain at various feedback currents.

The performance of the LNA is compared to other designs in Table 6. The proposed

LNA achieves the lowest NF both at room temperature and cryogenic temperatures with wider bandwidth and an order of magnitude better FoM compared to other designs.

Table 6 Performance comparison.

Reference	This work	[115]	[116]	[117]	[118]
Frequency (GHz)	**0.3-15**	DC-12	3-10	0.1-14	3-10
Gain (dB)	**37.3**	15	17	12.4	12.5
NF (dB)	**1.8-2.2** **0.74-1.26 (78K)**	2.3-4.5	3.5-4.3	2.7-3.7	3-7
OIP3 (dBm)	**+10**	+16	-	+8.6	-
Reverse isolation (dB)	**>44**	>24	-	>35	>45
Power (mW)	**52**	26	14.4	14.4	7.2
FoM	**35.4**	2.19	2.36	3.7	1.9
Area (mm^2)	**0.46**	0.38	0.15	0.134	0.64
Process	**130 nm SiGe**	130nm CMOS	65 nm CMOS	130nm CMOS	90nm CMOS

$$FoM\left[\frac{GHz}{mW}\right] = \frac{Gain.BW_{3dB}[GHz]}{(NF_{avg}-1).P_{DC}[mW]}$$

5.2.4 Summary

A wideband SiGe LNA was presented which achieves the lowest NF and highest gain-bandwidth product among the published state-of-the-art LNAs within a similar frequency band. The LNA utilizes a simple and efficient methodology for gain control. The performance of the LNA was measured over temperature and at cryogenic temperatures and the amplifier achieved a record average NF value of 1.0 dB over 15 GHz bandwidth with more than 39 dB of gain at 78 K. It was found that two physical mechanisms counteract each other by changing the temperature, resulting in robustness over temperature.

5.3 Single-Event Effects on W-Band Down Conversion Mixer

5.3.1 Introduction

There is a growing interest in utilizing millimeter-wave (mmW) frequencies (30-300 GHz) for satellite communications, space-based radars, radiometry, space exploratory probes, and landing systems. W-band radars are particularly interesting for cloud sensing satellites [44]. The 94 GHz cloud sensing profile radar (CPR) instrument was used in the CLOUDSAT spacecraft, launched in 2006 [45], [46].

Because of the reduced wavelength at this high frequency range, W-band radar enables higher resolution radar systems for safe and precise landing on planetary bodies. Radar offers a superior solution for landing systems due to its ability to operate at any time of the day, weather and through dust and engine plumes, as well as its ability to detect velocity coherently [47].

High frequency mmW radiometers and radars have also recently been utilized in Cubesats for atmospheric sounding and scientific applications. Because of the extensive space-based applications, it is crucial to understand the behavior of these high frequency systems under the radiation intensive conditions present in space.

SiGe BiCMOS technology is one of the best candidates for mmW applications [121], [122]. This technology offers higher yield and integration, with competitive speed compared to III-V technologies. It provides both high-speed SiGe HBTs and digital CMOS on the same platform. It is known that SiGe HBTs can operate over a wide range of temperatures, with improved performance at lower temperatures [22]. In addition, it is

known that these devices are inherently tolerant to high levels of total-ionizing-dose (TID) radiation [52], [123], [124]. However, SiGe HBTs exhibit sensitivity to single-event effects (SEE), as a result, for example, of high energy particle collisions. Therefore, a thorough study and understanding of SEE phenomena is crucial to predict the SET behavior and to design proper hardening schemes for the circuits implemented in SiGe technologies [3], [55]–[57], [125].

SEE on standalone devices, as well as digital and simple analog circuits, have been studied in the past. However, there is limited research on SEE in high-speed RF circuits [1], [4], [58]–[60], [126]. The reported circuits are typically operating around a few GHz and only include linear circuits. SEE in high frequency mmW circuits, as well as nonlinear RF cicruits and full receiver has never been investigated. In the present study, we investigate the SEE on a mmW SiGe front-end components and full front-end receiver for the first time.

A two-photon absorption (TPA) laser has been found to be a very useful tool for studying single event transients [127]. It has been demonstrated that the transients induced by such laser strikes can be representative of transients generated by heavy ion strikes [128],[129]. Therefore, TPA laser pulses were used in this work to induce transient carriers on different SiGe HBTs within the circuits in order to assess the impact of SETs.

5.3.2 Down-Conversion Mixer

The block diagram of W-band radar front-end is shown in Figure 90. The front-end consists of two paths, for transmit and receive, with a shared antenna. The received signal from the antenna is first amplified using a low-noise amplifier (LNA) and then is

fed to a down-conversion mixer. This signal is called the radio frequency (RF) signal. The RF signal consists of the desired data modulated on top of a high frequency carrier. The down-conversion mixer translates the high frequency input signal to a lower intermediate frequency (IF) to extract the modulated data. This can be accomplished by multiplying the received signal with a locally generated signal, the local oscillator (LO). The frequency of the resultant signal is equal to the difference between the frequencies of LO and RF signals. The resultant signal can then be amplified with lower frequency amplifiers and can be converted into a digital signal for further signal processing.

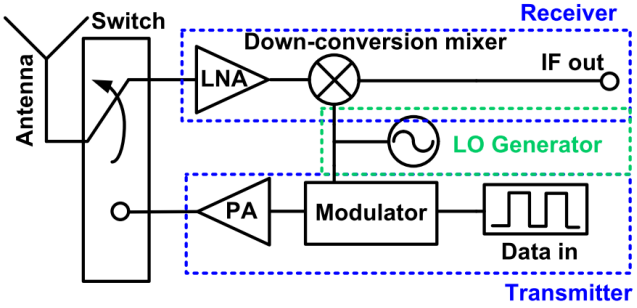

Figure 90. Simplified block diagram of the W-Band radar front-end.

In general terms, the basic operation of a down-conversion mixer is to multiply the RF signal by the LO signal and filter the resultant output signal. To operate with low LO power and good port to port isolations, a double- balanced active mixer configuration was selected. The schematic diagram of the designed mixer is shown in Figure 91. This topology is often utilized for the implementation of high performance transceivers. The circuit has two symmetrical differential branches and consists of two main parts as highlighted in the figure. The g_m SiGe HBTs (Q_1 and Q_2) are being used to amplify the received signal and provide isolation between the RF and LO ports, while the switch SiGe HBTs (Q_3-Q_6) are used for multiplication. The switch SiGe HBTs are alternatively turning

ON and OFF by applying the LO signal and alternate the path of the RF signal to the output of the mixer. The biasing current mirror, which mirrors 4 times the current into the g_m transistors is also shown in this figure.

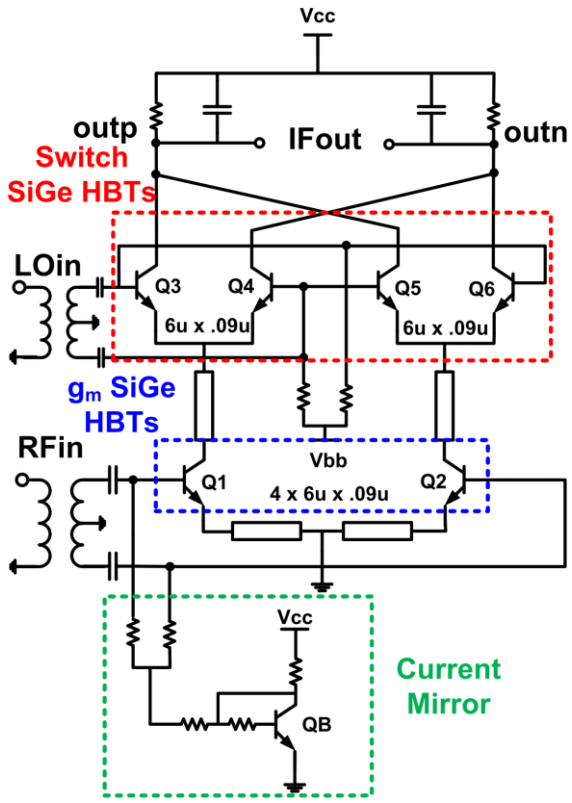

Figure 91. Schematic diagram of the W-Band down-conversion mixer.

Figure 92 shows the fabricated photomicrograph of the mixer. The circuit was implemented in IBM 90 nm technology (IBM-9HP) with f_T/f_{max} of 300/350 GHz, respectively.

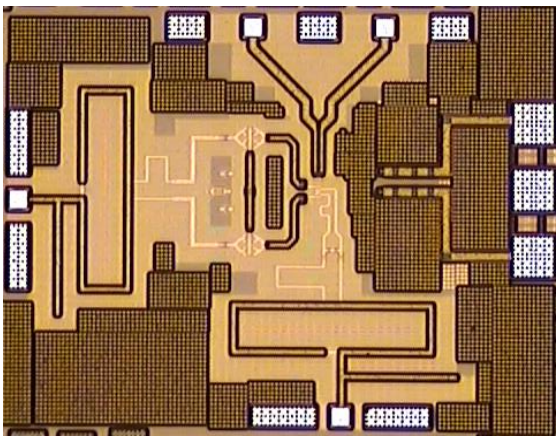

Figure 92. Die micrograph of the W-band down-conversion mixer.

Figure 93 shows the measured conversion gain and linearity of the circuit under normal operation point and under weak saturation conditions where Q1 and Q2 are partially enter the saturation region. This condition allows better tolerance to heavy ion radiation effects. Although operation under weak saturation conditions lowers the speed of devices, the f_{max} of the devices remain high enough that performance of the circuit was negligibly affected.

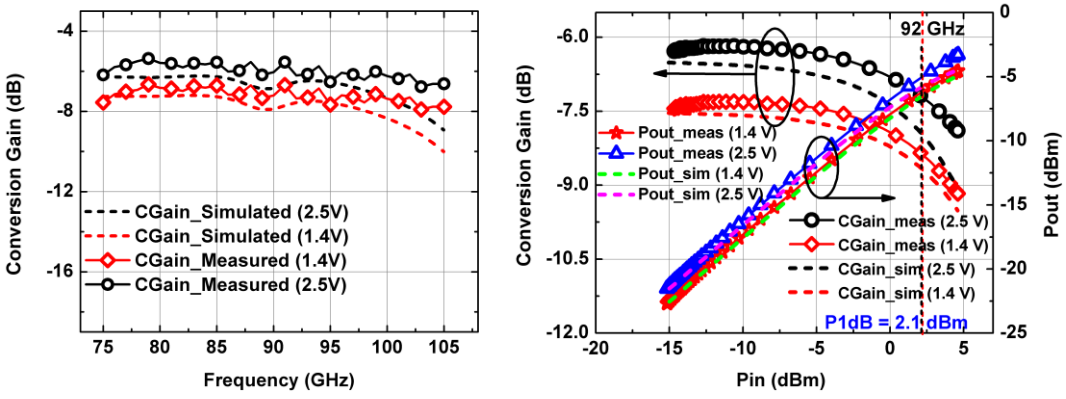

Figure 93. Measured conversion gain compared to simulation in two operating modes. (left), measured linearity compared to simulations. (right)

Figure 94 shows the measured IF bandwidth of the circuit as well as the measured performance of the mixer with respect to applied LO power.

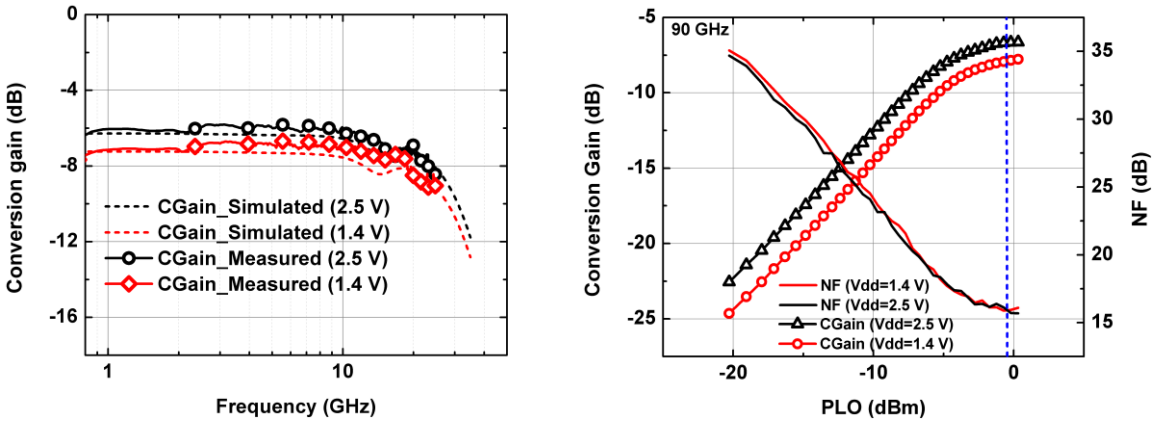

Figure 94. Measured conversion gain versus IF frequency compared to simulations in two power modes. (left). Measured conversion gain versus the applied LO power. (right).

The measured performance of the mixer is shown in Table 7. The mixer achieves 6 dB of conversion loss with only 0 dBm of the applied LO power and features high operational bandwidth, with more than 25 GHz of IF bandwidth.

Table 7. Measured circuit performance.

Measured Performance	This work	[22]	[23]	[24]
Frequency (GHz)	75-110	57-65	77	75-120
Conversion Gain (dB)	-6	+6.2	-10.3	-10
Required LO power (dBm)	0	0	+10	+7
Input P1dB (dBm)	2.5	-4.7	-8	-
LO to RF Isolation (dB)	38^{+}	30^{+}	30^{+}	41.5
IF Bandwidth (GHz)	25^{+}	1	1	24
Power Consumption (mW)	19.7	13	22	24

5.3.3 Theoretical Analysis of Single-Event Transients in the Down-Conversion Mixer

The down-conversion mixer can be considered a linear time-variant (LTV) system. Since the SiGe HBTs are turning ON and OFF very quickly, it is crucial to understand the dynamics of the circuit during single event transients (SET), as well as the propagation of transients to the output of the circuit.

Since the circuit in Figure 91 is symmetric, with a differential configuration, one can consider only one-half of the differential topology to simplify the analysis. Suppose that a current spike is generated at the collector of Q1 by striking a heavy ion on Q1. Transistors Q3 and Q4 are switching rapidly, with the frequency of LO which is 94 GHz in this case (every 10.6 ps). At one instant, Q3 is ON and Q4 is OFF, and as a result the transient current finds a path to the output (outp) of the mixer through Q3. At another time instant, Q4 is ON and transient current makes another path to the output (outn) while Q3 is OFF. This happens periodically, with the period of LO signal. Based on this description, it can be considered that Q3 and Q4 transistors are sampling the transient current at each time instant. This is demonstrated graphically in Figure 95. In this figure, only a half branch of the double-balanced mixer is shown for simplicity. Now we can use sampling theory to analyze the behavior of this time variant circuit in the presence of single event transient. Without loss of generality, let us assume that the heavy ion strike has created a current pulse at the collector of Q1 with an ideal pulse shape. Here we only consider the collector transient currents for the analysis. The effects of transient charges on the other SiGe HBT terminals can be found in a similar way and linear superposition can be applied to find the total transients at the output. The analysis will be performed for the single-ended output to cover the other mixer topologies which uses single-ended configuration. In addition, the

ideal pulse shape was chosen for simplicity of analysis. Nevertheless, the results can be

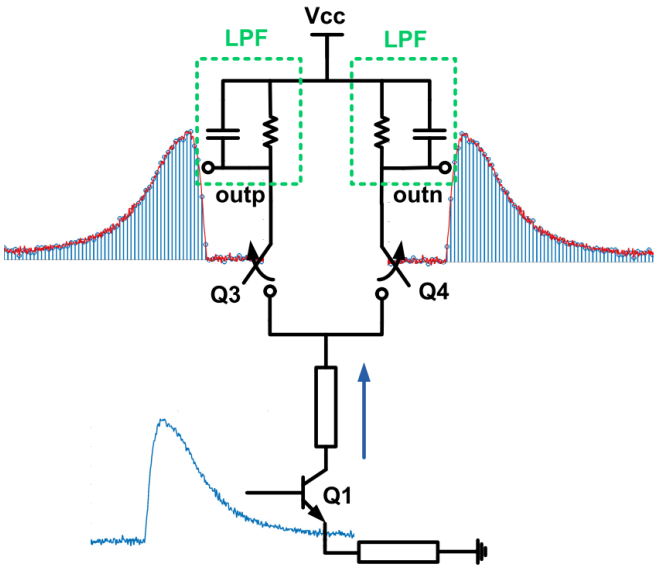

Figure 95. Transient pulse sampling with mixer operation.

applied to any other pulse shape. The time domain pulse and its frequency domain representation are shown in Figure 96. The figures here only show the normalized waveforms; nevertheless, the conversion gain of the mixer would change the height of the pulse at the output of the mixer. Now consider that the generated pulse is getting sampled by the Q3 and Q4 transistors to reach the output of the mixer.

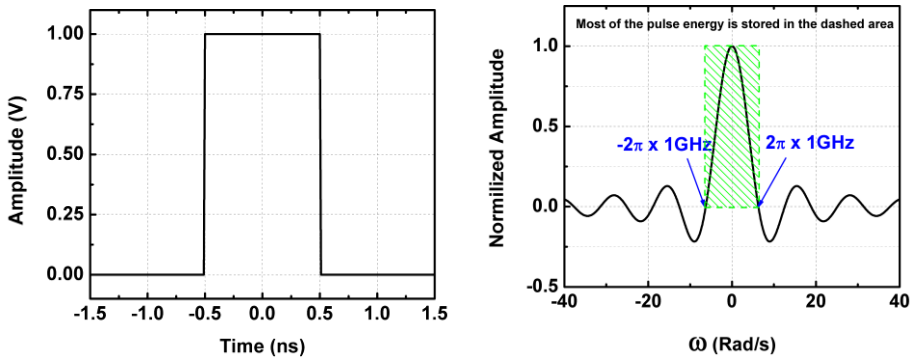

Figure 96. Ideal current pulse in time domain (left) and its frequency domain representation (right).

The continuous time-domain sampling can be represented as the multiplication of the train of delta functions by the pulse at sampling intervals [22].

$$f_s(t) = f(t) \times \sum_{n=-\infty}^{n=+\infty} \delta(t - nT_s) \qquad (18)$$

Here, $f(t)$ is the pulse function, $f_s(t)$ is the sampled pulse and $\delta(t)$ is the Dirac delta function. The Fourier representation of $f_s(t)$ can be found as follows.

$$F_s(\omega) = \frac{1}{T_s} \sum_{n=-\infty}^{n=+\infty} F(\omega - n\omega_s) \qquad (19)$$

$F(\omega)$ is the frequency domain representation of the $f(t)$. Based on Equation 19, the resultant frequency domain representation of the sampled pulse ($F_s(\omega)$) can be found by repeating the frequency response of the single pulse at multiples of the sampling frequency, as depicted in Figure 97.

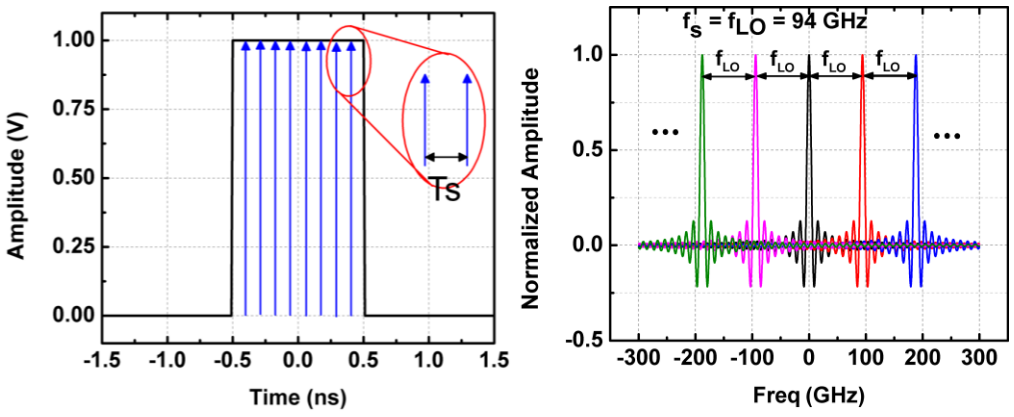

Figure 97. Time domain sampling representation (left) and frequency domain response (right).

The output IF port of the mixer utilizes a low-pass filter (LPF) to suppress the LO and RF leakages to the IF port. By applying this LPF to the waveform of the sampled

current, one can easily see that the original pulse shape is obtained at the output of the mixer. This is shown in Figure 98, where the LPF (blue) only passes the part of the waveform that is in its pass-band, and rejects the rest. The filtering leaves the original transient pulse shape at the output of the mixer. This shows that the original pulse shape is propagated to the output of the mixer with the same shape, while the switch transistors are periodically turning ON and OFF.

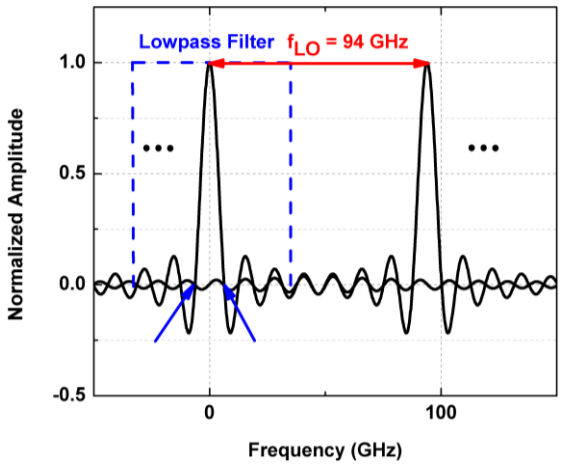

Figure 98. Frequency domain representation of the sampled pulse waveform.

This can be understood by considering the time domain operation of the circuit as well. The combination of the switch SiGe HBTs and the LPF work as a sample-and-hold at the output to reconstruct the shape of the single event transient. The switch transistors are sampling the transient waveform at each LO cycle and the output LPF holds the sampled transient up until the next cycle of LO and next sample.

It can be seen in Figure 98 that the original frequency response of the pulse can be reconstructed from the sampled pulse if and only if the repeated frequency domain responses do not interfere with each other. In this sense, the LPF can effectively filter out the original waveform without being altered by other repeated waveforms. The frequency

domain representation of the pulse contains most of its energy in its main lobe (Figure 96). To preserve the original pulse shape, these main lobes should not interfere with each other. By looking at Figure 98, this condition can be calculated as follows:

$$\boldsymbol{f_{LO} > \frac{2}{\tau}} \quad (20)$$

$$\boldsymbol{T_{LO} < \frac{\tau}{2}} \quad (21)$$

where T_{LO} is the period of LO signal and τ is the pulse width. Interestingly enough, this criterion is the well- known Nyquist criterion from the sampling theory which was expected.

In the time domain, this basically means that if the switch transistors are being switched at least a couple of times over the ion-induced transient pulse duration, the pulse shape will be propagated to the output of the mixer in the exact shape as it was generated. This has important implications in understanding the transients in the mixer and the entire receiver. This observation also shows that the generated pulse at the output of the mixer will not be altered by applying the LO signal. This means that the propagated transient to the output of the mixer will experience the same waveform regardless of the applied LO signal. This becomes extremely important for the laser experiment, since providing a mmW LO signal to the circuit during the laser experiment is extremely challenging. It is worth mentioning that this only holds when the applied LO period is at least a couple times shorter that the generated transient spike by the ion strike (Equation 20-21). In other words, for lower frequency RF mixers with a low LO frequency, the generated pulse shape might not propagate to the output of the mixer with the exact same shape and the transient response may depend on the instant of the ion strike. It is also worth mentioning that if the LPF at

the output of the mixer has a narrower bandwidth than the bandwidth of the generated transient, it would cause an exponentially decaying behavior in the propagated transient waveform in both cases.

Another way to understand the transient propagation to the output of the mixer is through the conventional mixer analysis. Let us consider the mixer operation as multiplying the current of each branch by a sequence of 1's and 0's as a result of the applied LO signal. The differential output can then be obtained by differencing the two outputs.

The Fourier series representation of the pulse train can be calculated as follows:

$$\boldsymbol{f(t) = \frac{\tau}{T} + \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{n\pi\tau}{T}\right) \cos\left(\frac{2n\pi}{T} t\right)} \qquad (22)$$

τ is the pulse duration and T is the time period of the pulse train. Based on the above representation, one can see the DC term conducts the low frequency SET directly to the output of each branch without up-conversion. As it will be explained in the next sections, by striking the g_m SiGe HBT, this DC term produces a common mode transient, which can be eliminated in differential topologies; however, the strike on the switch SiGe HBT produces a differential transient which cannot be eliminated.

In order to verify this theoretical analysis, we performed circuit simulations using the compact models of the SiGe HBT provided by the IBM foundry. Current pulses were applied in these simulations to resemble the generated current spikes from the heavy ion strike. Charge collection occurs at the different terminals of a SiGe HBT upon an ion strike; however, since the circuit is linear, superposition can be used to take the rest of the transient currents into account. The effect of only one ion-induced charge source will be shown in the following simulation. A more accurate and comprehensive TCAD simulation will be

conducted in the next section with a physical model of the device. Figure 99 shows the simulation setup and Figure 100 compares the transients observed at the output of the mixer when the LO signal is present with transients observed when an LO signal is not applied. Two different cases were simulated using different LO frequencies to validate the derived criterion.

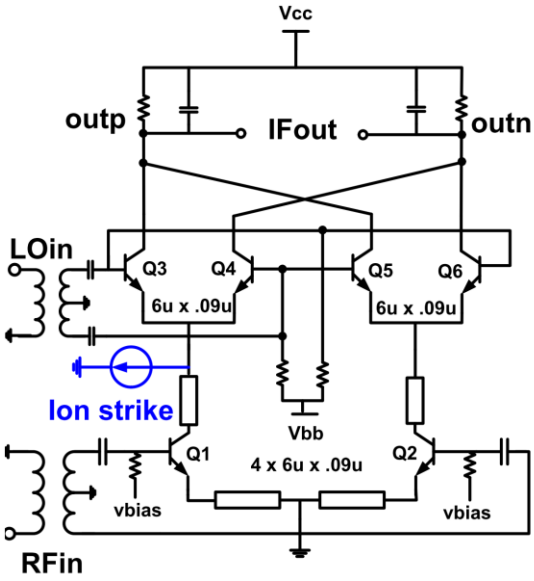

Figure 99. Pulse injection technique to simulate the SET effect.

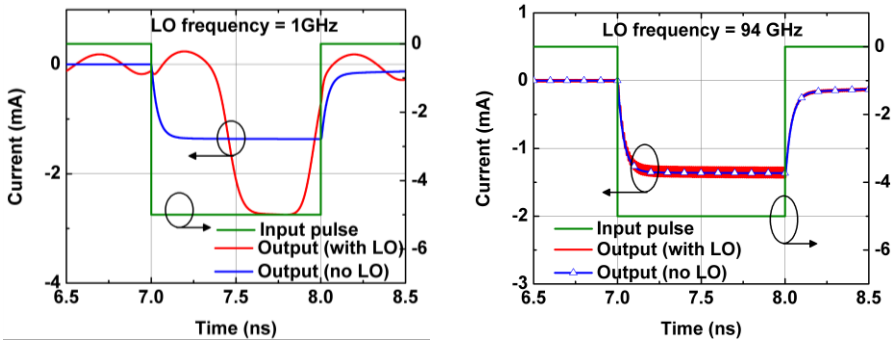

Figure 100. Simulation result comparing the output transients as a result of heavy ion strike when the LO signal is applied with the case when LO signal is absent. The LO frequencies are 94 GHz (right) and 1 GHz (left).

The first simulation considers the real operational frequency with an LO of 94 GHz, while the second case considers a lower LO frequency (1 GHz) that violates the criterion

derived earlier in Equation 20-21. As we can see from these figures, for the simulation with an LO of 94 GHz, the generated pulses at the output of the mixer are similar, regardless of the applied LO signal, as expected (Figure 100 (right)), while the pulse shape changes at the output of the mixer with lower LO frequency, which violates the criterion. This simulation proves the claims made in our analysis. These findings suggest that one can capture the single event transients at the output of the mmW mixer without applying the LO signal. This is a very important observation that will facilitate the transient experiment of very high frequency mixers and receivers.

It is worth mentioning that the high frequency signal present on top of the pulse in Figure 100 is the result of LO leakage to the IF port, and can be effectively filtered with IF LPF. A 1 pF capacitance was considered in the simulations at the IF port in both cases to help filter part of this LO leakage for more clarified demonstration of the actual pulse shape. In the real experiment, the IF port experiences extra parasitic components, including the cable, input capacitance of the oscilloscope as well as wirebond inductance, which form a LPF at the IF port and causes longer transients with an exponential shape at the output.

5.3.4 Sentaurus device level simulations

The circuit-level simulations using compact models in the previous section were very helpful to understand the dynamics of the SET propagation throughout a complicated LTV system. We considered current pulses that resemble those generated by ion-induced electron-hole pairs within the device upon a heavy-ion strike. However, in order to obtain more accurate physical behavior of the circuit and the dynamics of the generated electron-hole pairs by actual heavy ion strikes, mixed-mode TCAD device-level simulations were

conducted as well which will be described in this section.

To construct the physical device within the Sentaurus software, the SiGe HBT device test structures were characterized first, and DC Gummel and AC f_T / f_{max} characteristics were measured. This data was imported into the simulator to calibrate the device structure, the base current recombination velocity, base-collector doping and Ge profile at base. This insures that the device TCAD model closely matches the real device. Figure 101 shows the structure of the SiGe HBT with emitter length of 6 μm and width of 100 nm, and with CBEBC contact configuration. Figure 102 and Figure 103 compare the Gummel characteristics and f_T / f_{max} of the TCAD simulation with the measured data.

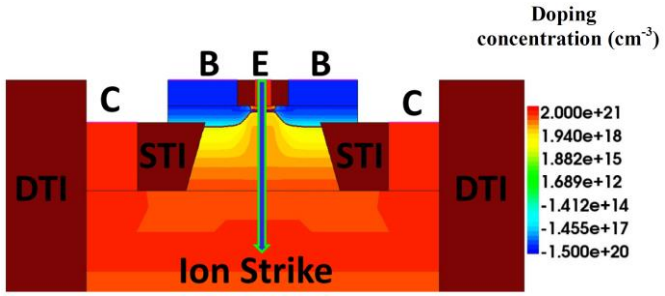

Figure 101. 2D structure of the device in Sentaurus.

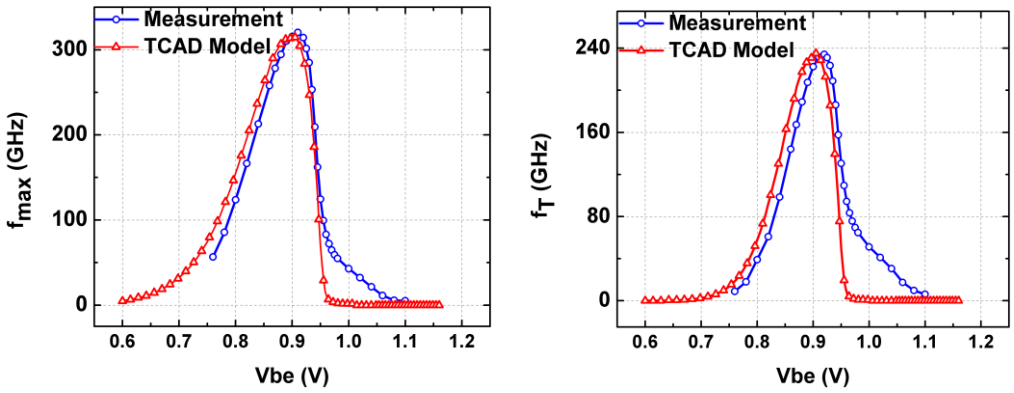

Figure 102. f_{max} of TCAD model compared to compact model (left), f_T of TCAD model compared to compact model (right).

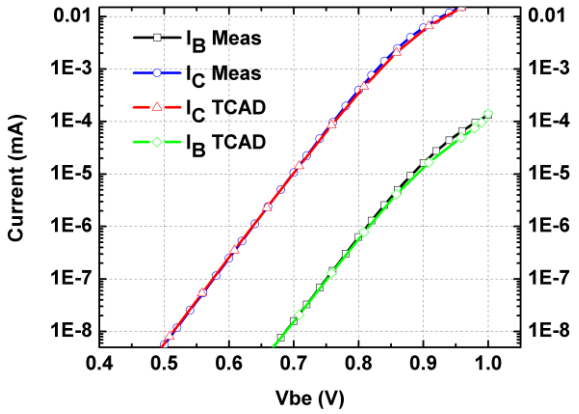

Figure 103. Gummel characteristic of TCAD model compared to measured data.

A close agreement between the simulation and measurement can be observed verifying the accuracy of the designed model. Transient mixed-mode TCAD simulations were utilized to find the SET response at the output of the mixer. Figure 104 shows the generated output transient current by striking the Q1 transistor for the strike with an linear energy transfer (LET) of 0.216 MeV . cm2 / mg, and compares two cases, with and without an applied LO signal.

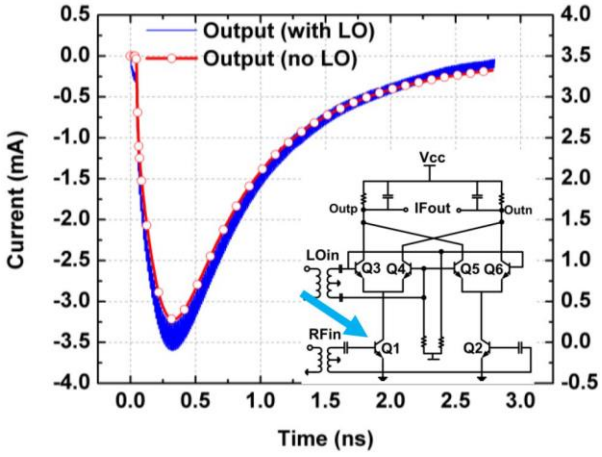

Figure 104. SET simulation results using Sentaurus.

As we can see from this figure, a considerable current pulse is generated at the

output of the circuit which lasts for several nanoseconds. The figure also shows that the generated pulse current at the output of the mixer is essentially the same, regardless of the LO signal, except the high frequency leaked LO signal to the output as explained earlier, similarly proving the analysis results in the previous sections. However, some discrepancies with the measurement results are expect since the laser energy is not exactly known. In addition, extra parasitic components at the output of the circuit due to the cable, wirebond, PCB PADs and oscilloscope input capacitance have not been considered in this simulation.

5.3.5 Experimental results and discussion

The fabricated die was mounted on a custom-made PCB, which was specifically designed to allow the backside substrate of the die to be exposed for laser irradiation. Laser-induced transients were measured at the U.S. Naval Research Laboratory (NRL) using carrier injection by through-wafer, two-photon absorption (TPA) using 150 fs optical pulses with a less than 0.9 μm FWHM charge distribution profile (in silicon). This system enables 3-D, position-dependent, time-resolved measurements of single-event transients (SET). The two IF outputs of the mixer were monitored using a broadband, real time oscilloscope to observe the laser-induced transients. The block diagram of the TPA laser testing setup is shown in Figure 105, [130].

Long transient tails of SET may not be a concern in digital circuits, but they are certainly a big concern in RF applications. Since this high frequency mixer processes very high data rates or very narrow radar pulses, the presence of a long transient tail can potentially corrupt multiple bits of data or the short pulses of a radar signal. However,

because of fully differential configuration of the utilized double balanced mixer, the strike on a g_m SiGe HBT produces a common-mode transient current, and thus the differential signal extraction can potentially eliminate this transient at the output.

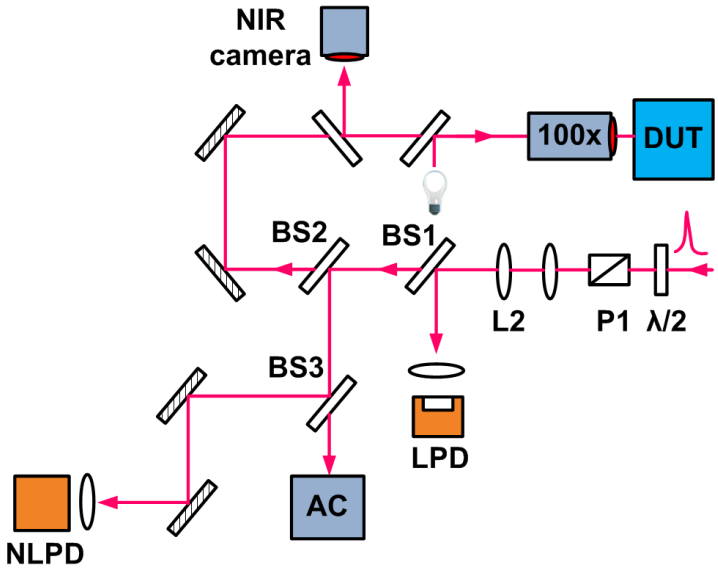

Figure 105. Block diagram of the TPA laser system. LPD is the InGaAs linear photodiode, NLPD is silicon nonlinear photodiode, AC is autocorrelator, L2 is collimating lens, λ/2 is a half-wave plate, P1 is calcite polarizer, BS1-BS3 are beam splitters, and 100x is the microscope.

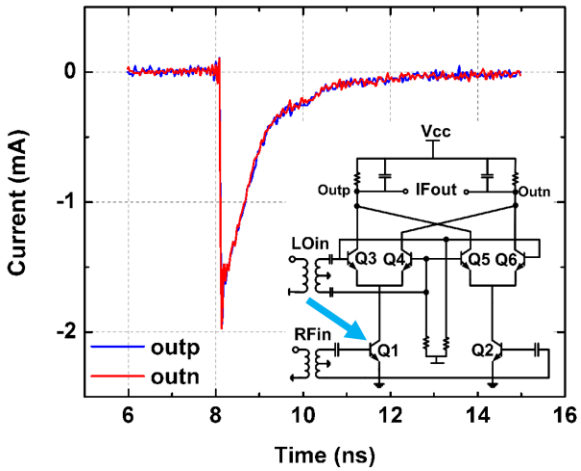

Figure 106. Transient current measured at the output (outp, outn) of the mixer for the strike on one of the gm HBTs.

To study the SETs at the output of the circuit, each of the SiGe HBTs were struck with the laser. The generated transient current pulse at the outputs of the mixer due to the strike on one of the g_m SiGe HBTs is depicted in Figure 106. Figure 107 shows the differential transient at the output of the circuit. One can see that the differential signal has suppressed the transient current at the output considerably. This is an important observation that would suggest utilizing fully differential architectures for mixers in order to suppress the transients of g_m SiGe HBTs. Clearly the full transients will appear at the output of the mixer topologies which do not utilize differential configuration. It is worth mentioning that although the effective differential signaling suppresses the net transients at the output of the mixer, the presence of strong transients (although in common-mode) may still effectively saturate the high gain IF amplifiers downstream in the signal path from the down-conversion mixer. This can also result in the corruption of the received data.

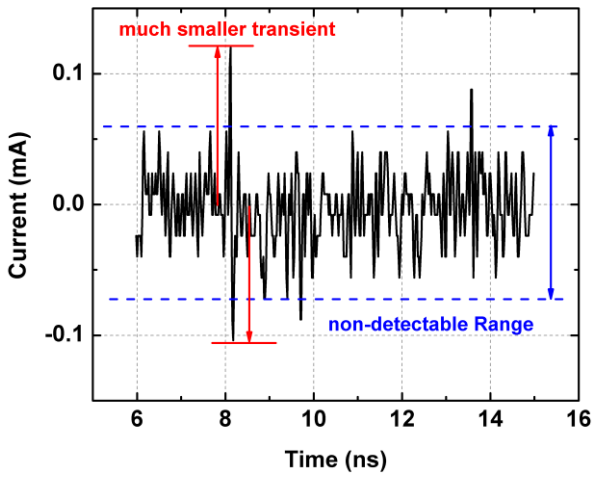

Figure 107. Differential transient currents at the output of the mixer as for the laser strike on the gm SiGe HBT.

To determine the sensitive areas of the device, the active area of the same g_m SiGe HBT was scanned with laser beam strikes with fine steps of 0.5 μm. The resultant transients at the output of the circuit were captured and recorded with the real-time oscilloscope.

Figure 108 shows the 2-D raster scan of the peak transient currents produced at the output of the mixer. The 1-D cut of the raster scan of

Figure **108** along the X-axis is shown in Figure 109. Based on these data, we can see that strikes on the emitter of the g_m SiGe HBT produce the biggest transients at the output of the circuit.

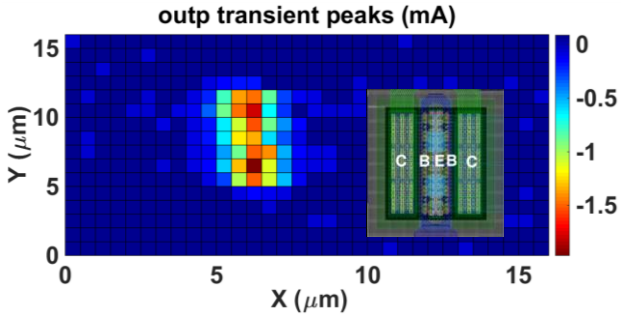

Figure 108. 2-D transient peaks at the output of the mixer for the strikes scanned over one of the gm SiGe HBTs.

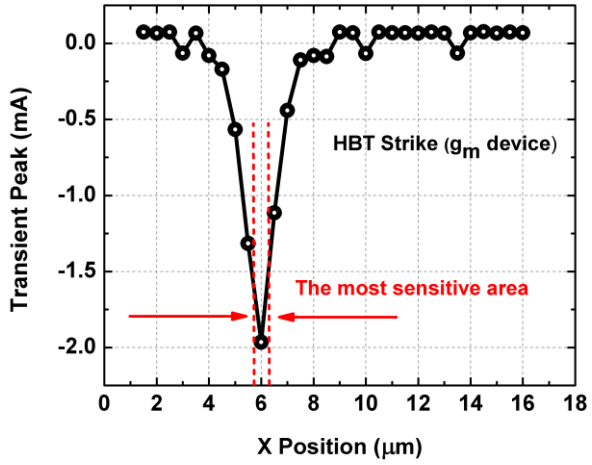

Figure 109. Measured transient peaks by scanning the laser across one of the gm SiGe HBTs with the layout configuration shown in

Figure 108 at Y = 6 µm.

A similar experiment was conducted on one of the switching transistors of the mixer. The transient response of the circuit due to the laser strike on the switch device is shown in Figure 110. The switch transistor does not produce a common-mode transient, as opposed to the g_m transistor. In fact, the emitter-coupled topology of the switch acts like an active balun to produce a differential transient at the output of the circuit. This can be observed in Figure 110. Therefore, the net transient current at the output is bigger for the differential topology. In other words, once the Q3 transistor is struck with a laser beam, electron-hole pairs are generated in Q3, which result in a transient current spike at Q3. Since the sum of the currents of Q3 and Q4 is fixed and is determined with biasing current of Q1, any increase in the current of Q3 will produce a similar reduction in the current of Q4. This causes a differential transient to appear at the output of the circuit. Compared with the transient current of the g_m SiGe HBT, the switch transistor produces much smaller transient currents; however, the settling time of the resultant transient is longer than that of g_m SiGe HBT. Part of this smaller transient arises from the fact that the g_m SiGe HBT acts as high impedance degeneration to the switching SiGe HBT, and thus most of the laser-generated carriers within the switching SiGe HBT cannot easily flow to the output of the mixer, and therefore recombine. The generated transient, however, is much larger than the typical detected signal at the receiver, and can effectively result in the corruption of the multiple bits of the received data.

Figure 111 shows the 2-D plot of the peak of the transient currents at the output of the mixer due to the laser-induced transients on a switch SiGe HBT and Figure 112 plots

the Y cut of the 2-D laser scan over the device, identifying the most sensitive regions of the SiGe HBT.

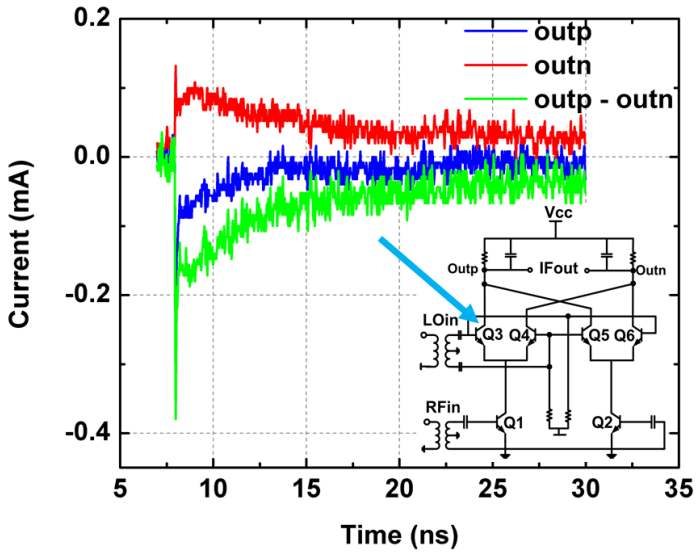

Figure 110. Transient current measured at the outputs (Outp, Outn) of the mixer for the strike on one of the switching SiGe HBTs.

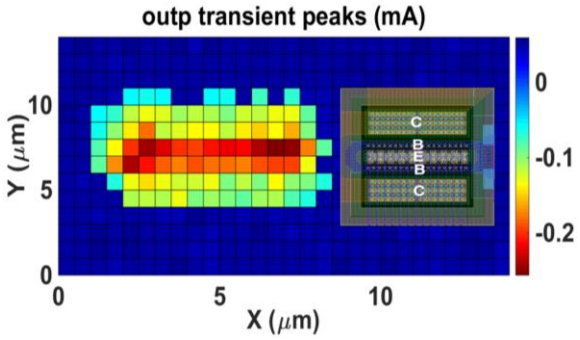

Figure 111. 2D output transient peaks at the output (Outp, Outn) of the mixer for the strikes scanned over one of the switch HBTs.

Finally, the current mirror SiGe HBT device (Q_B) was struck by the laser. The generated transient current at the output of the mixer is depicted in Figure 113. This transient has a longer settling time compared to the g_m SiGe HBT transient. This can be explained by examining the circuit schematic in the same figure. Because of the presence of the large resistors connected to the current mirror SiGe HBT, the time constant at the connection

nodes of this SiGe HBT is larger, producing a longer settling time. This transient can be reduced some by lowering the mirroring ratio to allow higher current at the mirroring SiGe HBT, at the expense of more DC consumption. Furthermore, since the transient from the

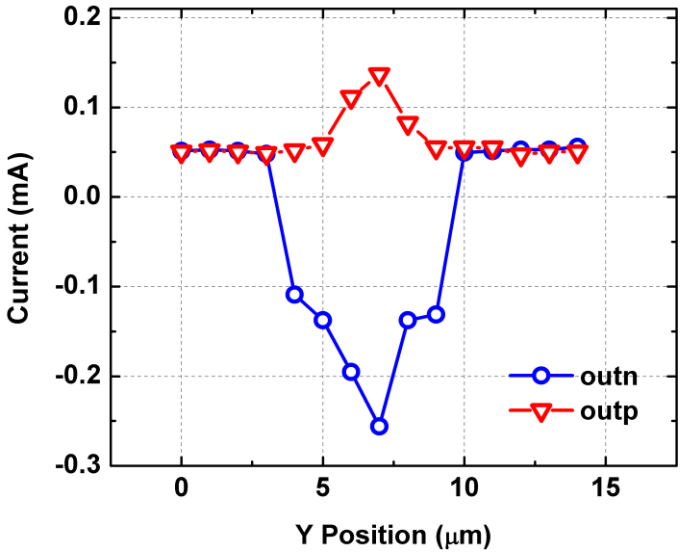

Figure 112. Measured transient peaks by scanning the laser across one of the switch HBTs with the layout configuration shown in Figure 111 across X = 6.5 μm.

current source is also a common-mode signal, similar to the g_m SiGe HBT transient, the resultant differential signal at the output, suppresses the transient at the output of the mixer. This common-mode transient can saturate the IF amplifier, however, even for a high linearity IF amplifier.

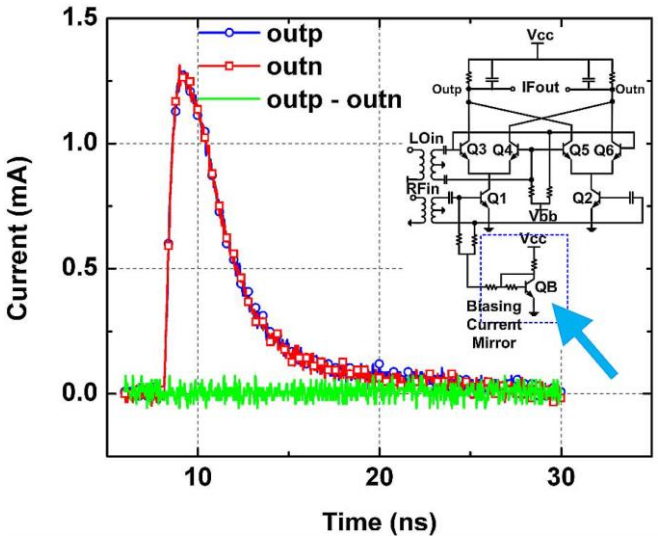

Figure 113. Transient current measured at the output (Outp, Outn) of the mixer for the strike on the biasing current-mirror SiGe HBT.

5.3.6 Summary

SETs were investigated in a W-band radar down-conversion mixer. The propagation of the transient pulse throughout the complicated linear time-variant circuit was analyzed. It was shown that the transient currents propagate to the output of the mixer regardless of the applied LO signal if and only if the mixer switches at least twice during the single event transient. Circuit and device simulations were conducted to prove this theory. A through-wafer laser experiment was also conducted to induce the transients at different SiGe HBTs and capture the SETs at the output of the mixer. It was shown that a differential topology can effectively mitigate some of the transients at the output of the mixer.

5.4 Single-Event Effects in High-Frequency Linear Amplifiers

Single-event effects on a nonlinear switching RF circuit was studied in previous section. The results from previous section, clarified the SET properties and propagation inside RF receivers. In this section, theoretical and experimental studies on linear RF amplifiers will be covered. Modelling and simulation strategies proposed in this section agrees closely with experimental data and provides a fast and accurate strategy for simulating more complicated high frequency circuit and systems. In addition, it was shown that linear circuits theory can be utilized to provide useful insights for the circuit designers to choose more SET tolerant topologies and to design proper techniques to mitigate these effects.

5.4.1 X-band Low Noise Amplifiers

Two SiGe LNAs were designed and implemented in 130 nm bulk SiGe process technology (GlobalFoundries 8HP) to study the sensitivity of the amplifiers to SETs. Both LNAs cover the X-band frequency range for a targeted radar application.

The first LNA utilizes resistive feedback topology. The details of the design can be found in section 5.2.2 of the current chapter (see Figure 84 and Figure 85). It provides more than 37 dB of gain in a wide frequency range of 0.3-15 GHz, with less than 1.8 dB of NF throughout the entire bandwidth. The second selected topology for this study is the emitter degenerated topology. This topology is widely utilized in RF transceivers. Two LNAs at L-band and X-band were designed using this topology for the current study. These LNAs have bandpass characteristics centered at X-band and L-band respectively also referred as tuned amplifiers. From this point forward, the emitter degenerated amplifiers will be referred as tuned amplifier and the resistive feedback amplifier will be referred as wideband amplifier.

The schematic of the tuned amplifiers at X-band and L-band are shown in Figure 114. These amplifiers were designed and implemented in the same 130 nm bulk SiGe technology as the wideband amplifier (GlobalFoundries-8HP). The size and biasing of SiGe HBTs were designed in such a way to achieve simultaneous noise and power matching for better sensitivity and power gain at the same time. The core of these amplifiers was also realized using a cascode configuration with multiple parallel fingers. This allows a proper comparison point between the wideband amplifier and tuned amplifier. The resistor at the upper base terminal and the resistor at the collector resonator were incorporated for stability reasons. Both amplifiers use a single stage emitter degenerated topology. The L-Band LNA was particularly designed to achieve low noise figure and

extremely small intermodulation products. Figure 117 shows this LNA achieves excellent OIP3 of higher than +25 dBm. The X-band amplifier achieves a low NF performance below 1.5 dB and provides a peak power gain of +14 dB.

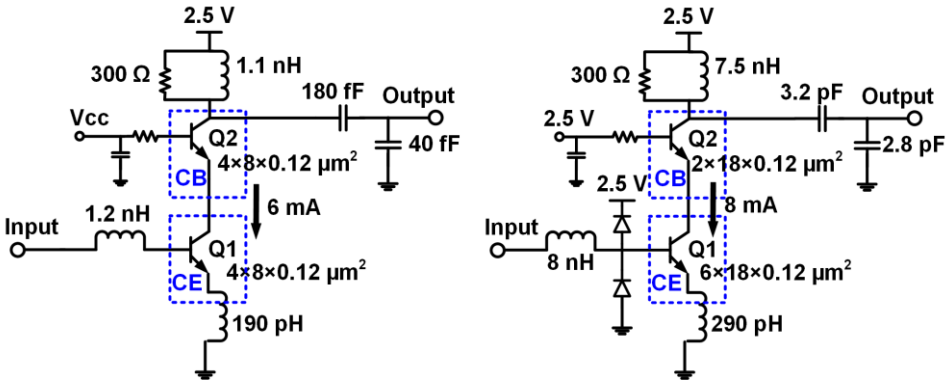

Figure 114. X-band LNA for X-band phased array radar (left), L-band LNA for NASA's GPS receiver.

Figure 115. shows the die micrograph and measured S-parameters of the X-band LNA. Figure 116 and Figure 117 show the die micrograph and measured performance parameters of the L-band LNA.

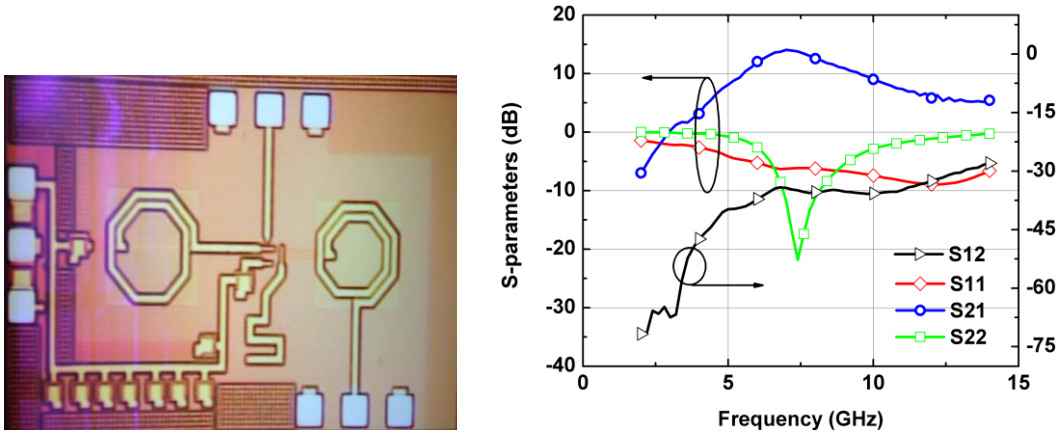

Figure 115. Die photo of the X-band LNA (left). Measured S-parameters (right).

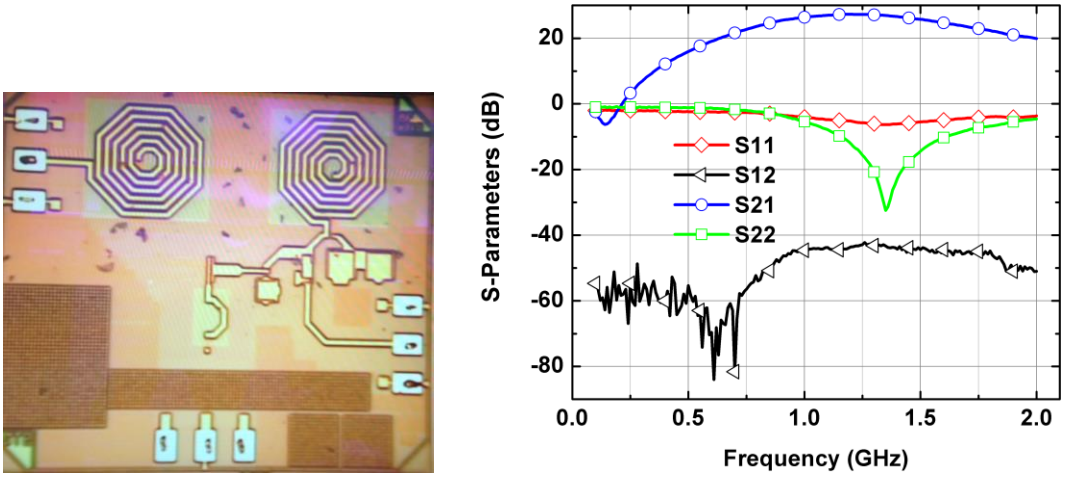

Figure 116 Die photo L-band LNA (left). Measured S-parameters (right).

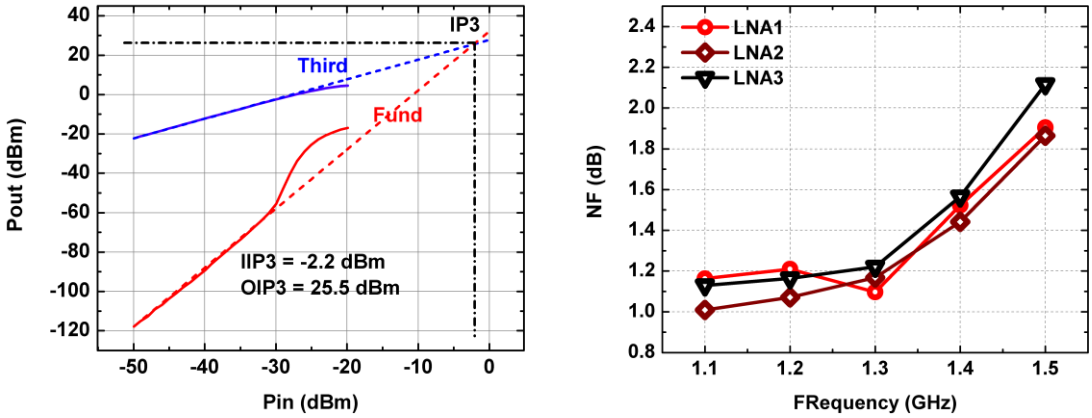

Figure 117. Measured 3rd order intermodulation intercept points (left). Measured noise figure of 3 different dies (right).

In the remainder of this section, the SET performance of the wideband amplifier and X-band tuned amplifier will be investigated as the test circuits which represent linear amplifiers. The SET behavior of the L-band amplifier follows a similar trend and will not be discussed here. Interested readers are referred to [3]. Both X-band and wideband amplifiers utilize the cascode topology as the core of the amplifiers. The inductive emitter-degenerated topology is a tuned amplifier, which can only provide amplification around a narrow range of frequencies centered at X-band, whereas the wideband amplifier provides

a wideband gain in a broad frequency range from 0.3 to 15 GHz. Clearly the time-constants of these amplifier topologies are different and that can play a major role in determining the SET behavior of these respective configurations. In addition, the wideband amplifier incorporates two amplification stages with higher power gain.

5.4.2 Simulation methodology

In the previous section, we utilized mixed mode device simulator where the complete physical structure of the device was created in Synopsys Sentaurus software in such a way that electrical performance of the model could closely match up with the measured performance of the device. These types of simulations can effectively provide the most accurate simulation of the effect of heavy ion strikes on standalone devices or relatively simple circuits. However, for large and complicated circuits, the simulation time becomes excessively long, with challenging convergence issues. In addition, it is difficult to incorporate the measured or electromagnetic (EM) simulated S-parameters of passive components directly into these types of simulators, unless it is being modeled by passive lumped elements. For these reasons, we propose to utilize a combination of the device and circuit simulations for accurate and fast simulations of the SET on the high frequency LNAs at the same time. Our approach in the current study utilizes charge injection technique which has been used in the past for circuit level SET simulations [131]–[133]. However, instead of using approximate models such as double exponentials, we utilize the device solver to estimate the SET charges generated in different terminals of the device. There are approximations involved in using this technique compared to the complete device level simulations which mainly comes from the impedances present in different terminals of the device within the circuit. In addition, part of the injected current flows into

the device itself when current injection technique is utilized and causes inaccuracies in predicting the resultant SET of the circuit. Nevertheless, these impedances can be incorporated within the device solver to obtain more accurate estimations. As an alternative, a more sophisticated sub-block can be simulated within the device solver instead of standalone device to obtain more accurate estimation. For instance, device simulations were performed on cascode configuration in the present study instead of standalone device to account for the non-grounded emitter terminal of the upper device (see

Figure **114**).

First, the structure of the device was constructed within the TCAD device simulator following the procedure outlined in the previous section [1]. Measured f_T/f_{max} data as well as DC Gummel characteristics were utilized to calibrate the device parameters by adjusting device structure, the base current recombination velocity, base-collector doping and Ge profile at base. This insures that the device model has the same physical structure as the fabricated device.

Since both LNAs use a cascode configuration, the ion strike simulation in TCAD was performed on the cascode topology and the transient currents at different terminals were captured for strikes on CE and CB devices. These terminal currents were then imported into the advanced-design-system (ADS) circuit simulator for simulating the transient response of the entire circuit. The simulated transient currents of the cascode from the Sentaurus device software was injected as current sources into the corresponding circuit nodes in the circuit (see Figure 118.). This technique provides the accuracy of the device

solver combined with the speed of the circuit simulator. In addition, it allows the straightforward modeling of the parasitics of the measurement setup, including connection cables, wirebonds, and oscilloscope loading effects within the circuit simulator. This technique can be used for fast SET simulation purposes of any circuit configuration. Figure 118 shows this simulation technique conceptually, along with the simulated terminal currents of the cascode topology from TCAD software upon ion strike simulation of a CE device.

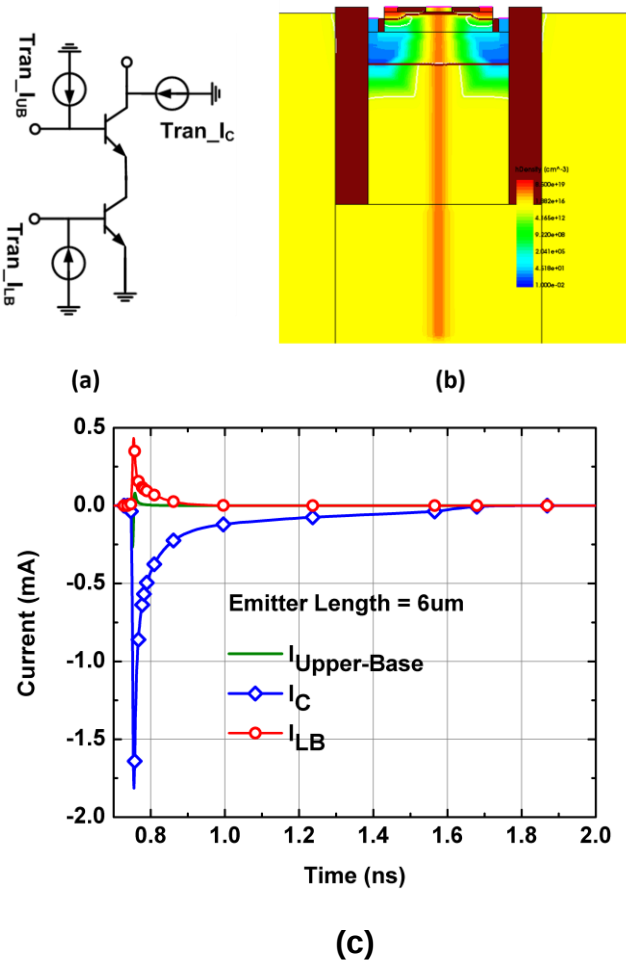

Figure 118. Current injection scheme (a), 2D structure of the device (b), and simulated transient currents upon ion strike on a 6 µm CE SiGe HBT (c).

To further emphasize the approximations involved in the proposed technique, let's consider the introduced inaccuracies in the current designs. There are two approximations involved in the current-injection technique which can result in inaccuracy in the prediction of the SET response of the circuit. First, the excitation ports within the device software do not include the actual impedances that are present in the circuit. Thus, it can cause inaccuracy in the generated transient currents from the device software. These impedances however, can easily be incorporated in excitation ports within the device simulator for more accurate simulations. In the present case, this effect was negligible, since the bottom emitter was grounded and the voltage at upper collector impedance had negligible effect on the resultant transient current due to negligible dependence of collector current to collector voltage. Furthermore, small impedances are located at base terminals.

Second, a small portion of the injected current within the circuit solver, can flow into the terminals of the device itself when used in circuit simulator. This can affect the resultant SET response of the circuit. This effect can also be compensated by adjusting the excitation port impedance in the device solver. However, in the case of cascode topology, either the device terminals have high impedance such as collector node, or the impedances seen from the terminals of the device toward the circuit is very small such as base terminals. In this case, only a small fraction of the injected charge flows into the device and does not cause significant inaccuracy.

5.4.3 Experimental results and discussion

To verify the modeling and simulation procedure, a TPA laser experiment was conducted at NRL. The fabricated die was mounted on a custom PCB board which was specifically designed to allow backside laser irradiation. Transients were induced in various devices by laser using carrier injection by through-wafer, TPA 150 fs optical pulses with a less than 0.9 μm FWHM charge distribution profile (in silicon) [130]. This system is particularly useful for studying the SET in complicated circuits since it enables striking each individual SiGe HBT with a focused laser beam because of the fine spatial resolution in controlling the laser beam location in 3D dimension as well as the small beam width. Compared to broad-beam heavy ion exposure with unknown strike locations, the TPA laser beam facilitates striking the desired locations within the circuit or even within the device [134]. The output of the circuit under laser irradiation was monitored continuously with a real-time high-speed oscilloscope to capture the generated transients at the output. The laser beam was focused on various devices by monitoring the beam spot using an infrared camera, and by performing a fine spatial scan across the device (with the resolution of tenths of microns). This was done by controlling the motorized precision stage to locate the active region of the devices (most sensitive spot within the devices). The height of the stage was then adjusted so that the largest SET was produced. This procedure was conducted for any individual device reported in this study.

Q1 SiGe HBTs (CE device) in both tuned and wideband amplifiers were struck with a focused TPA laser beam, and the generated SETs were captured at the output of the LNAs. Figure 119 compares the captured transient waveforms of the two LNAs. It was shown in section 5.3 that the produced SET from the circuit components within the receiver chain can propagate throughout the receiver, and ultimately corrupt multiple data bits [1].

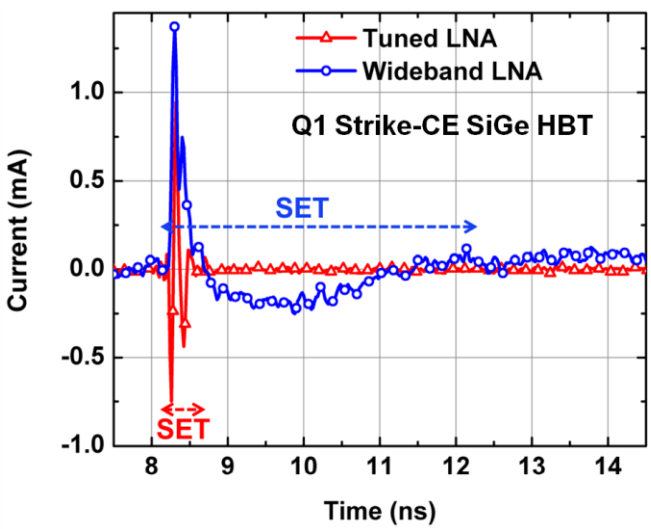

Figure 119. Measured SET response of the LNAs for the strike on the Q1 SiGe HBT (CE device).

It is worth mentioning that unlike digital circuits which are processing large signal data bits, the LNA and other RF front-end components are processing very low power signals captured from the antenna. Therefore, even the small tail of the SET in Figure 119 can easily corrupt multiple data bits in the receiver.

It can be seen from Figure 119, that generated SET at the output of the tuned X-band amplifier settles quickly while the SET of the wideband LNA lasts for a relatively long period of time. This is surprising, considering the wideband operation of the -resistive feedback LNA, one can expect relatively fast settling behavior for this type of amplifier. The settling behavior of linear circuits can be analyzed using well known circuit theories. For instance, impulse response or equivalently, the step response of the circuit can be used as a useful tool to analyze the settling behavior of the LNAs. This is particularly useful since impulse response and the equivalent frequency response of linear circuits are known

to circuit designers and can provide useful information about the SET behavior of different circuit topologies.

Let's assume that ω_H is the upper 3-dB cut-off frequency of the resistive feedback amplifier, and let's approximate this amplifier as a single pole system. The impulse response of this circuit for the input current excitation can be found by Equation 23.

$$\boldsymbol{h(t) = \lambda_H . \omega_H e^{-t.\omega_H}} \qquad (23)$$

Equation 23 shows that this circuit can settle down in a short period of time of approximately $\frac{5}{\omega_H} \approx 53\ ps$ (5 times of the time constant). This time period is much shorter than what was obtained from the experiment simulations. The long settling time of the circuit comes from another low frequency pole within the circuit. Further investigating the circuit in Figure 84 (previous section), one can see the presence of the relatively large decoupling capacitor in between the stages. Although this capacitor presents very low impedance at higher frequencies, it creates a low frequency cut-off frequency in the circuit and acts as like as high-pass filter. This low frequency pole creates a slow decaying exponential transient that we see from the measured data. Assuming that ω_L is the lower cut-off frequency of the amplifier, Equation 24 shows the complete impulse response of the circuit by including this low frequency pole.

$$\boldsymbol{h(t) = \lambda_L . \omega_L e^{-t.\omega_L} + \lambda_H . \omega_H e^{-t.\omega_H}} \qquad (24)$$

Simulations verify the effect of this low frequency pole on the slow decaying transient at the output of the LNA.

Figure 120 shows that the inclusion of de-coupling capacitor, creates a long transient tail at the output of the LNA.

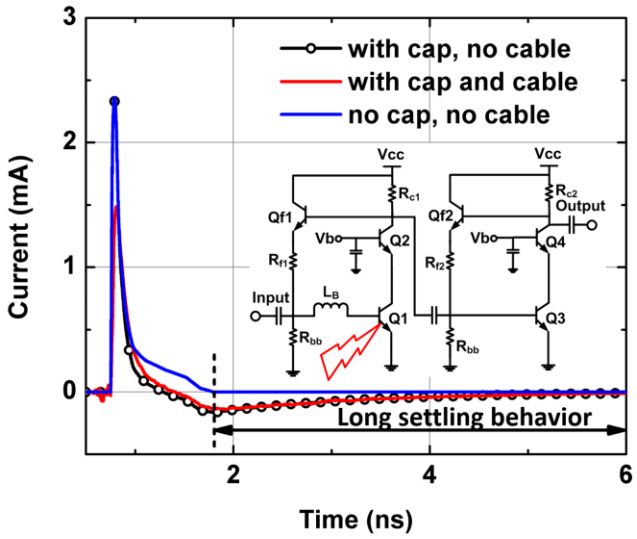

Figure 120. Simulated output transient current of the resistive feedback LNA showing the effect of de-coupling capacitor and cables for the excitation of the Q1 SiGe HBT (CE device). Inclusion of the cable attenuates the magnitude of SET and adds extra delay to the output SET. The SET response in this figure was shifted back in time for comparison purposes.

This is an important observation since the low frequency response of these types of LNAs are typically neglected for most of wideband applications such as UWB communication, however as we saw in this experiment, it plays a major role in SET response of the wideband LNA. This pole can be eliminated however by replacing the inter stage de-coupling capacitor with a DC level shifter circuit.

Although the impulse response analysis can only be used for moderate-energy strikes where the circuit is still operating in linear conditions, but it can still be utilized for analyzing the response of the circuits to SETs with reasonable accuracy. In addition, one can calculate the SET at the output of the circuit using time domain convolution formula (Equation 25 and Equation 26).

$$\boldsymbol{SET_{out}} = \sum_{i=1}^{i=n} \boldsymbol{SET_{device}(i) * h_i(t)} \quad (25)$$

$$\boldsymbol{SET_{out}(t)} = \sum_{i=1}^{i=n} \int_{-\infty}^{+\infty} \boldsymbol{SET^i_{device}(\tau) \times h_i(t-\tau)\, d\tau} \quad (26)$$

$SET_{device}\,(i)$, and $h_i(t)$ are attributed to transient currents at various terminals of the device, and associated impulse responses from those excitation ports on the device respectively. SET_{out} is the linear superposition of the resultant convolutions from various excitation ports. For very short SET pulses, or for low frequency circuits, however the resultant convolution (i.e the output SET) follows the shape of the impulse response approximately, when the SET of the device is much shorter than the impulse response of the circuit. To prove this, Figure 121 compares the simulated normalized impulse-response of two LNAs when the Q1 transistor (CE device) is excited with an impulse current. To calculate the impulse response of the circuits, the width of the excitation current pulse should be much shorter than the impulse response duration. In the current simulation, the width of the current pulse was 4ps.

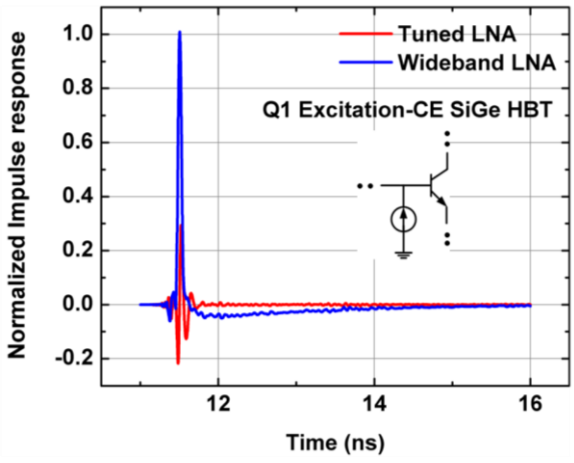

Figure 121. Comparison of the simulated impulse response of the LNAs for the excitation of the Q1 SiGe HBT (CE device). The impulse response is a unit-less function and in order to calculate that, the resultant output current was divided to

the excitation current pulse. The plots were normalized here to show the relative strength of the impulse responses between two different types of LNAs.

The effects of wirebonds and cables were incorporated in the simulation setup, this essentially lowers the bandwidth of the circuits and increases the duration of the time domain impulse response. In addition, the pulse width and amplitude of the excitation was adjusted such that the transient impulse response ($h(t) = \frac{output\ transient\ current}{input\ excitation\ current}$) becomes insensitive to the excitation pulse width and amplitude, this assures that the input can be considered as an impulse excitation. As we can see from this figure, the response is similar to SET response of the circuits depicted in Figure 119. Compared to laser experiment, where the high-gain wideband LNA provides compressed power-gain to large SETs, the simulated impulse response of the wideband amplifier provides higher power-gain for the small-signal impulse excitation. Nevertheless, for high energy ion strikes, the duration of the SET could be much longer than the impulse response of these high-speed circuits and in those cases the SET should be calculated following Equation 26. For SETs with much longer duration than the duration of the impulse response of the circuit, it is expected that the resultant SET at the output of the circuit follows the SET shape of the standalone device.

To further validate the results of linear approximation, impulse responses from different excitation ports for the strike on Q1 SiGe HBT of the resistive feedback amplifier were calculated using transient simulations. The output SET was then calculated numerically using the calculated impulse response functions, and the excitation currents from TCAD and utilizing Equation 26. Figure 122 compares the result of this linear approximation with the result of transient simulations for the strike on Q1 SiGe HBT of

the resistive feedback LNA. These results have good agreement with transient simulations, except than the peak transient value. As mentioned before, the amplifiers provide smaller gain to large signal excitations due to gain compression effects, therefore the peak current value is smaller compared to peak current value from linear approximation.

Figure 123 compares the captured output transient currents of two LNAs for the strike on Q2 (CB) transistor. Resultant SET at the output of tuned LNA once again decays faster compared to wideband LNA which includes a large de-coupling capacitor. In addition, the peak of this SET in CB device is much smaller than the SET generated from Q1 (CE) device shown in Figure 119. This can be explained by considering the cascode schematic shown in Figure 84 and Figure 114. The base terminal of the CB device is shorted to the supply (or includes very small resistance for stability reasons). The low impedance at base terminals provides a low impedance path to generated electron-hole

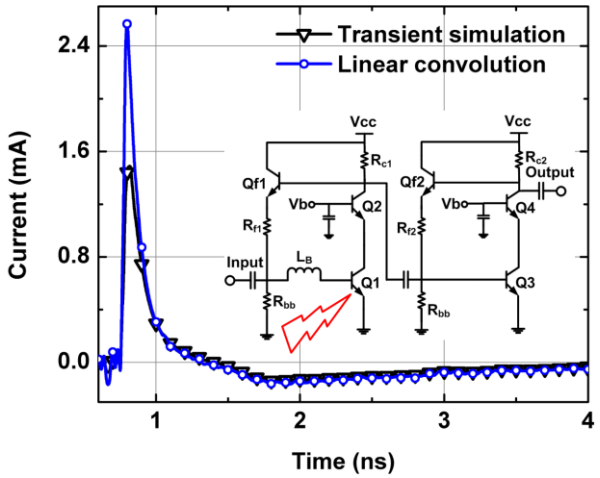

Figure 122. The simulated SET with linear approximation technique compared to transient simulation at the output of the resistive feedback LNA for the strike on Q1 SiGe HBT (CB device).

pairs to flow quickly out of the device. This can significantly reduce the peak of the generated SET. In addition, the CE device provides a considerably large impedance at the emitter terminal of the CB device, and therefore the extra charge carriers cannot easily flow from this terminal and must find another path or recombine within the device.

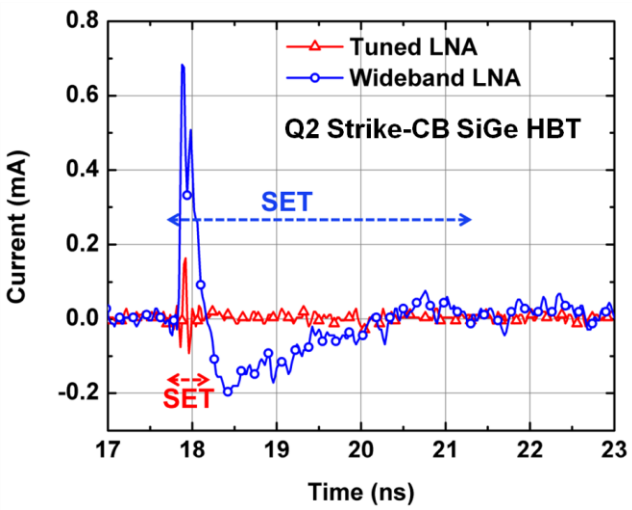

Figure 123. Measured SET response of the LNAs for the strike on the Q2 SiGe HBT (CB device).

To verify the accuracy of the proposed simulation methodology in section 5.4.2, Figure 124 compares the measured SET results of the wideband LNA for the strike on Q1 SiGe HBT with simulations.

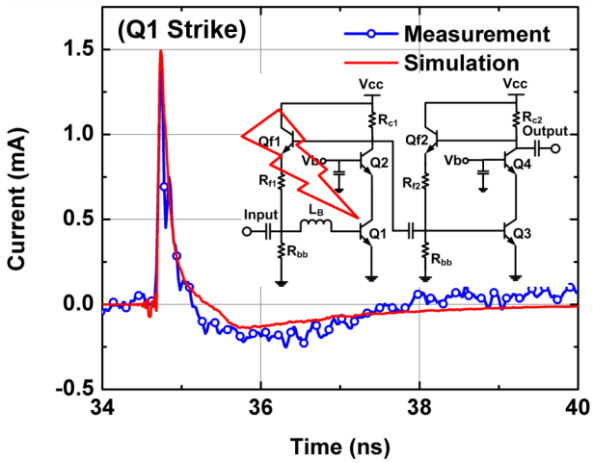

Figure 124. Comparison of the SET response of the wideband LNA with simulation for the strike on Q1 CE device.

The energy level for the ion-strike simulation was adjusted in the TCAD simulator so that it matches the generated peak from the experimental data. This energy level was then kept fixed for the rest of simulations across different devices within both LNAs. There is a good agreement between the simulation and measurement results. The discrepancy observed in Figure 124 for t > 38 ns is attributed to simulation approximations of the measurement setup, such as, wirebonds, transmission lines on printed-circuit-board (PCB), etc. The accumulated charge within the Q1 device is calculated as 0.44 pC for this particular simulation. Compared to some of our previous experimental data for the generated charge from heavy ion strikes, this value is reasonably close to the produced charges from heavy ion strikes. As an example, the measured accumulated charge from the device struck with Oxygen ions and with LET of 2.19 MeV.cm^2/mg was 0.29 pC. The measured accumulated charge for the strike with Neon with LET of 3.49 MeV.cm^2/mg was about 0.38 pC, and for Argon (LET=9.74 MeV.cm^2/mg), it was approximately 1pC.

As another example, Figure 125 compares the measured and simulated results for the strike on the Q2 device of the tuned X-band LNA (CB device). Once again, a good matching between the measurement and simulation can be observed from this figure, proving the accuracy of the models and simulation approach.

Accurate modeling and fast simulation capability of the SETs which are in close agreement with the experimental data, allows the comprehensive simulation of the effect of various components within the circuit, which can facilitate the design of radiation hardening techniques. The fine spatial resolution of the laser beam allows taking a precise raster scan over the circuits and even devices to highlight the most sensitive areas.

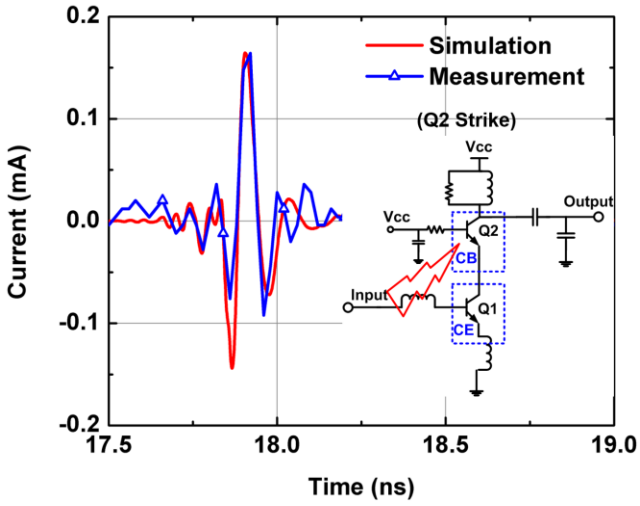

Figure 125. Comparison of the SET response of the X-band LNA with simulation for the strike on Q2 device (CB device).

Figure 126 shows the measured 2-D raster scan of the peak transient currents produced at the output of the wideband LNA for the strikes on the Q1 (CE) SiGe HBT, which consists of four parallel SiGe HBTs. One can observe that center part of the devices

are the most sensitive spots for SET. This part is the active region of the SiGe HBT device with vertical configuration which produces the highest transients.

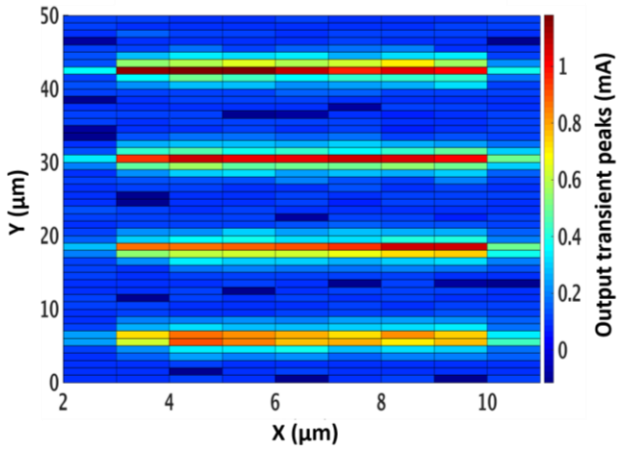

Figure 126. 2-D transient peaks at the output of the resistive-feedback LNA for the strikes scanned over the Q1 SiGe HBTs (CE devices). (Four SiGe HBTs in parallel). (See Figure 124).

To complete the study of the SET on resistive feedback LNA, further experiment was conducted to capture the SETs resulting from the other active devices within the circuit. Figure 127 shows the transient currents at the output of wideband LNA for the strike on feedback level shifter SiGe HBT. Although the amplitude of the resultant transient current is relatively smaller than the produced SETs for the strikes on other SiGe HBTs in the first stage, this SET level is still much stronger than the received signal at the input of the receiver and can completely corrupt the received data. To get a sense of the signal power level at the input of the receiver, one may consider that the power level of the received data is often close to the input noise floor of the receiver.

Figure 128 and Figure 129 show the produced SETs for the strikes on the SiGe HBTs of the second stage of the wideband amplifier. These transients are clearly much

smaller than the resultant SETs from the first stage. This result was predictable since the SETs from the first stage are being amplified with the second stage of the amplifier. Once again, the simulation results closely match the measured data. In addition, similar to the SET response of the first stage, it can be seen again that SET on CB device is much smaller than SET on CE device.

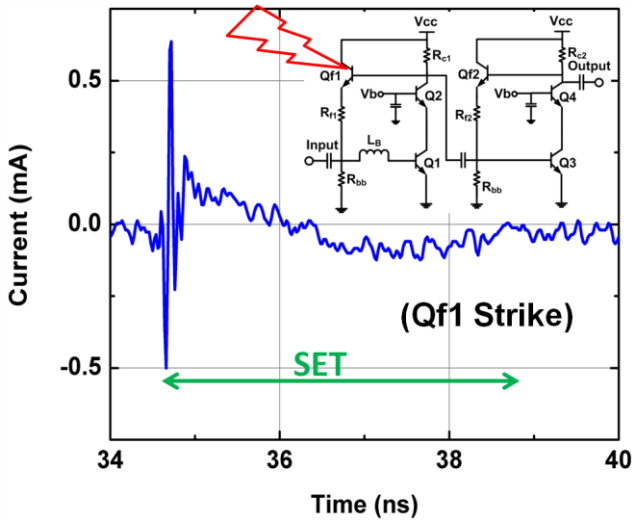

Figure 127. Transient current measured at the output of the resistive-feedback LNA for the strike on the feedback SiGe HBT.

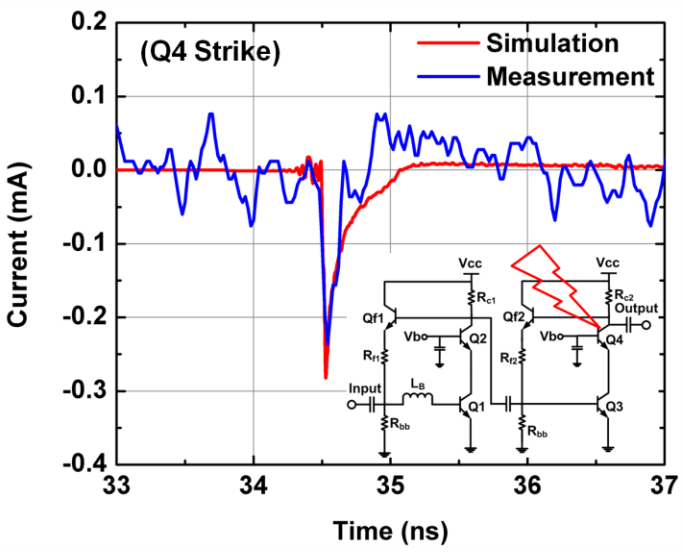

Figure 128. Transient current measured at the output of the resistive-feedback LNA for the strike on the Q4 SiGe HBT (second stage) compared to simulation.

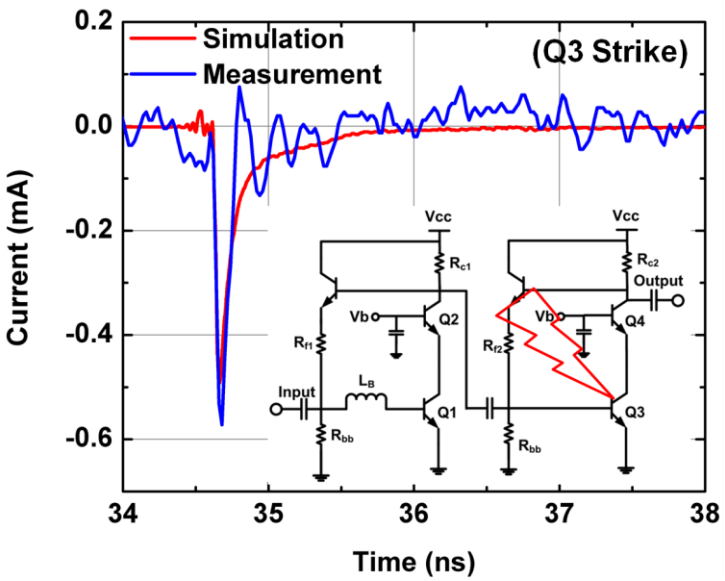

Figure 129. Transient current measured at the output of the resistive-feedback LNA for the strike on the Q3 SiGe HBT (second stage) compared to simulation.

5.4.4 Summary

The SET behavior of two commonly used low noise amplifier topologies were investigated in this study. Two SiGe X-band LNAs were designed and implemented in advanced 130 nm SiGe process for this purpose. SETs were induced in various devices within the LNAs using TPA laser pulses with 150 fs optical pulse width and less than 0.9 μm FWHM charge distribution profile. The structure of the device was designed within TCAD device software, and extensive combined device and circuit level modeling and

simulation were performed. A close agreement between the simulation and measurement was achieved for these high frequency RF circuits. The techniques presented in the present study can essentially be used for any other types of circuit configurations for SET modeling. In addition, it was shown that well-known impulse-response and convolution theory can be utilized for analyzing the settling behavior of the circuits in the presence of SETs and to identify less SET-sensitive circuit topologies.

CHAPTER 6. SINGLE-EVENT EFFECTS IN A MILLIMETER-WAVE RECEIVER FRONT-END

6.1 Introduction

In the previous chapter the SET behavior of linear amplifiers and down-conversion mixer was studied. A framework was established for modeling and simulation of SETs in sophisticated circuits with high accuracy and high speed. The transition of SET throughout the nonlinear switching mixer was understood and analyzed. TPA laser experiments were conducted to prove the proposed concepts. The results of the experiments show a close agreement between modeling, analysis and simulation with experimental data. These types of studies were conducted for the first time in the context of high frequency RF and mmW circuits, and paved the way for understanding, modeling, simulation and experiment on sophisticated circuits such as RF transceivers. In this chapter, the SET behavior of a millimeter-wave receiver will be studied. A novel methodology was proposed that allows the SET investigation in high frequency receivers. Additional high frequency circuits were implemented in the same chip as the mmW receiver to facilitate on-chip signal conditioning and processing. It was shown how SET study of high frequency circuits can be accomplished by including the laboratory equipment inside the same chip as circuit under test and incorporating the lab-on-chip concept. The proposed technique enables bit-error-rate (BER) measurement of the entire receiver at frequencies as high as mmW frequencies. Modeling and simulations were conducted following the methodology proposed in the previous chapter. In addition, a TPA laser experiment was conducted on the mmW

receiver. The results of experiments were in close agreement with simulations. This is the first study on investigation of the effects of SET on entire mmW receiver.

6.2 High Frequency W-band Receiver Front-End and Testing Procedure

The block diagram of a typical W-band transceiver front-end is shown in Figure 130. In transmit mode, the front-end switch connects the antenna to the transmitter output while isolating the receiver from the antenna. The digital data is then modulated on top of the high frequency carrier generated by a local oscillator (LO) unit and transmitted after amplification by a power amplifier (PA). In receive mode, the front-end switch connects the antenna to the receiver while isolating the antenna from the transmitter. The received signal from the antenna is first amplified with a low noise amplifier (LNA), and then demodulated with the down-conversion mixer to recover the digital data from the mmW carrier signal.

The main challenge for testing each individual circuit in this mmW sub-system comes from the difficulty in providing mmW external LO and RF signals to the circuit under test. Although a more sophisticated waveguide packaging may be utilized to feed the circuit from external mmW sources, the required waveguide packaging precludes the circuit from TPA laser pulses and is not compatible with standard TPA laser testing system.

The other difficulty comes from the fact that these high-frequency tuned circuits generate extremely short pulses upon ion strike which cannot be directly captured with existing real-time oscilloscopes. Therefore, it is impossible to study the radiation effects on the individual high frequency circuit blocks with existing measurement capabilities.

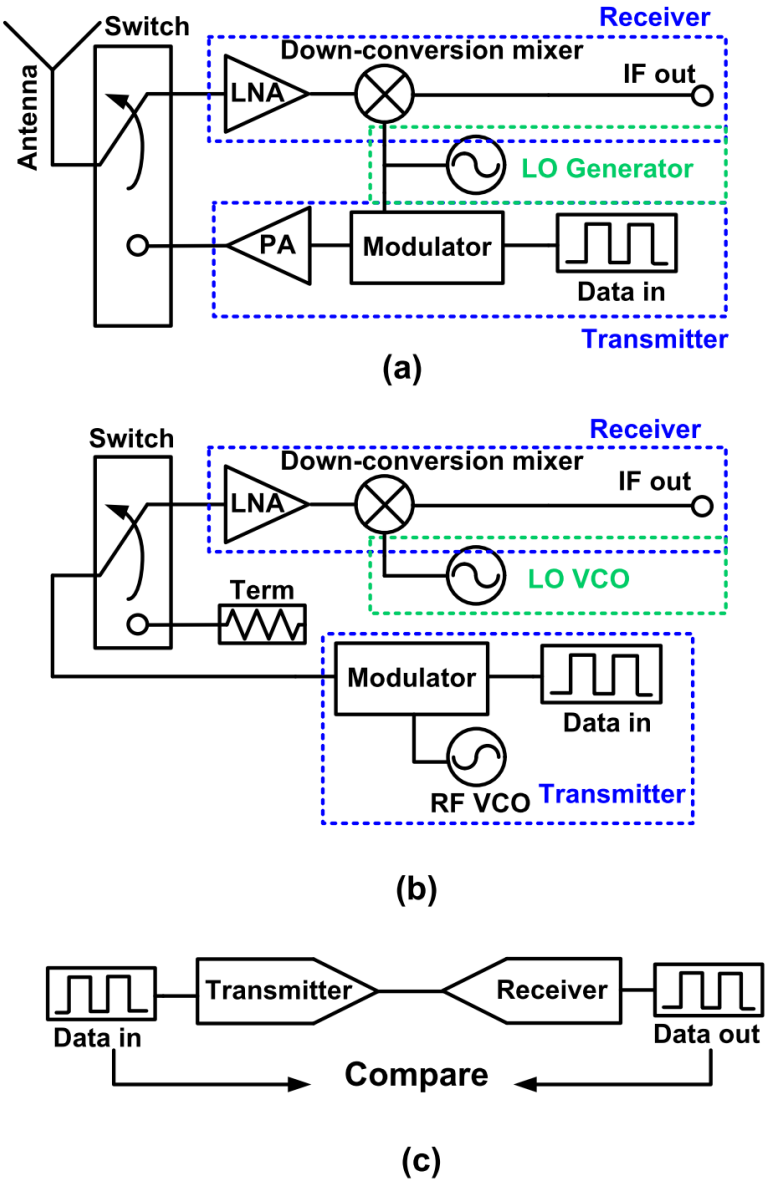

Figure 130. Simplified schematic block diagram of the W-band transceiver (a), block diagram of the proposed circuit module for SET testing (b), and simplified block diagram of the proposed scheme (c).

The solution proposed in the current study utilizes on-chip circuit components instead of external laboratory equipment. Thus, high frequency components required for the present testing was implemented on die with the receiver, in order to prevent the need for any external mmW instruments. In addition, the entire receiver chain as well as full data modulation and demodulation circuitries were also implemented on-die. The

generated short pulses from the high frequency circuit components propagate throughout the receiver chain and expanded after passing through low pass filters at IF port [1]. By applying an input digital data to the system, the effect of the expanded transient on the demodulated data can now be easily captured and characterized. Furthermore, standard SET calculation metrics such as BER can be utilized.

The block diagram of the proposed scheme is shown in Figure 130 (b). The circuit has been implemented in a 90 nm, 300 GHz SiGe platform (Global Foundries SiGe 9HP).

The low frequency digital data was fed to the input of the transmitter. The data was modulated on top of an 83 GHz RF carrier which was designed and implemented on-die. The modulated data (output of the transmitter) was then fed directly to the input of the receiver. At the receiver side, the input data (output of the transmitter) was first amplified by a low noise amplifier (LNA) and passed to down-conversion mixer for demodulation. Another on-chip LO source was designed to feed the down-conversion mixer. This source was utilized to demodulate the detected signal at the output of the LNA using the down-conversion mixer. This process extracts the digital data from the carrier which is a standard process utilized in direct conversion receivers.

In other words, the entire transmitter and receiver chain was designed and implemented on-chip including modulation and demodulation circuitries. The output of the transmitter was directly connected to the input of the receiver (see Figure 130 (c).). Digital data was fed to the input of the transmitter and modulated signal at the output of the transmitter was fed to the receiver input. The receiver demodulates and recovers the same digital data. This allows one to run SET experiment on the full system, compare the input

data to the transmitter with the received data at the output of the receiver and capture the effect of transients on the detected data at the output of the receiver. This allows one to calculate the bit error rates, identify the most SET-sensitive components, and design proper SEE hardening schemes to mitigate these effects.

SET sensitivities of various components of the receiver and transmitter including on-chip signal sources were captured by shining the TPA laser beam on constituent transistors. In the current study, we focus on the measured SET results of the front-end LNA and mixer (i.e., the mmW receiver) as proof-of-concept cases to show the effectiveness of this new methodology, to establish the SET sensitivity of the receiver sub-system, and to identify the sensitive nodes of individual components while the data is being processed through the receiver chain.

The high frequency modulator in Figure 130 was designed using switches inside the RF VCO. The modulator bypasses or passes the VCO signal depending on the applied digital input to perform ON-OFF-Keying (OOK) modulation on top of the 83 GHz carrier signal. For statistical analysis, it is preferred to apply a pseudo-random bit stream (PRBS) as digital input signal; however, due to lack of the high frequency PRBS generator, a deterministic sinusoidal tone was used as a digital input. Here, the positive cycle of the tone defines a logical “1” and the negative cycle defines logical “0”. For TPA laser testing purposes, and based on the proposed architecture shown in Figure 130 (b), one can either apply an external data stream to the modulator input or simply shift the RF frequency away from the LO frequency by Δf_{RF}. In the latter case, the down-converted signal would have a single frequency tone at a frequency of Δf_{RF} resembling a modulation of a tone with the

frequency of Δf_{RF} on top of the carrier generated using the former modulation method. In this study, both techniques for modulation and data extraction were utilized.

6.3 Simulation Methodology

Since the presented system consists of multiple circuit blocks, simulating the entire unit in a device-level simulator is extremely challenging, if not impossible. Therefore, the proposed methodology in the previous chapter which was using a combination of device and circuit simulations was utilized for modeling and simulation of this system.

The goal in the present study is to understand the propagation of SET within the receiver chain and effects of SET on the received data stream. Simulation results of the effect of the SET on the detected data bits at the output of the W-band receiver front-end will be demonstrated in the current section. The measured experimental data will be demonstrated in the following section. Following the traditional circuit simulation approach, the entire circuit was modeled in ADS simulator. Each circuit component within this simulation setup utilizes the foundry provide compact models of the transistors. The rest of the interconnections, transmission lines and other passive components were EM simulated and imported into the simulation test bench. The parastics of the measurement setup such as cables, connectors were measured and were included in this simulation. The length of wirebond connections were estimated and modeled in the simulations. A 5 Gbps pseudo random bit stream (PRBS) was modulated on top of an 83 GHz carrier signal and fed into the input of the W-band receiver in the present simulation (see Figure 130. b and c). ON-OFF Keying (OOK) type of modulation was used to modulate the 83 GHz carrier. The same modulation scheme was implemented on-die.

Figure 131 shows the results of the transient simulations and the effects of the ion strike on the recovered data at the output of the receiver. This figure includes the comparison between the recovered digital data at the output of the receiver with the input digital data which was fed to the transmitter modulator. The receiver circuit correctly demodulates and recovers the data. The detected data stream with and without the presence of SET is presented in this figure as well. For the present simulation, the simulated transient currents from the TCAD software, were injected into one of the bias devices of the LNA to simulated the generated SET currents. This simulation utilizes the full circuit components of the receiver front-end.

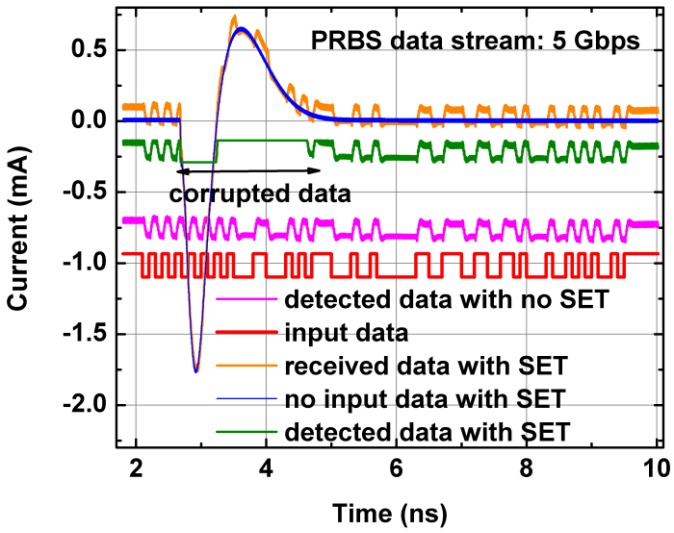

Figure 131. Simulation results of the effect of SET on the detected data bits at the output of the receiver front-end for the simulated ion strike on bias transistor of the LNA.

The presence of SET affects multiple data bits at the output of the receiver. In addition, this simulation shows the recovered digital data following the decision circuitry where the signals above a certain threshold are considered as logical “1” and data bits below a certain threshold are considered as logical “0”. One can see that SET causes

multiple erroneous bits at the output of the receiver. Compared to SET effects on digital circuits, many more data bits can be lost in RF receivers upon the SET occurrence. The present simulation and testing considers exaggerated high RF power in the receiver. The received power can be considerably lower; thus, many more data bits can erroneously be detected in real situations. The transient waveform of the SET at the output of the receiver while no input data is applied, is also shown in Figure 131. One can see that the SET is essentially sited on top of the recovered digital data with the exact same shape when there is no input data applied to the system. This is another important observation from this simulation which indicates that generated SET is propagated throughout the receiver, and directly sits on top of the recovered data bits. This observation is verified in the next section with experimental data.

6.4 Experimental Results and Discussion

As explained in the previous chapter, there are various techniques that can be used to simulate the effects of high energy particle strikes on the circuits. Broad-beam heavy ion exposure is the most realistic method being used in this regard [53], [54], [129]. However, the location of the ion strikes is random and unknown in this method, and thus doesn't allow a thorough study of the radiation effects on individual circuit blocks or devices. Some research institutions utilize ion micro-beam exposure to cope with this limitation; however, the ion energy of such beams can be too low to simulate the effects of heavy ion strike [128],[54]. Irradiation with lasers beams represent another technique to generate electron-hole pairs within the standalone device, which allows the study of SETs in both devices and circuits [127],[135],[136]. Accurate control of the strike location is the main advantage of this technique compared to other techniques. The strike location can be controlled within

tenths of micrometers, allowing one to not only produce the transients in any desired device, but also to scan the device itself with the laser beam and determine the sensitive locations of the device. In addition, the laser energy is controllable and can be monitored over the time. Since the mmW radar circuit has multiple complex circuit components, this technique is well suited for our experiment to study the sensitivity of the mmW components within the receiver to SET. Nevertheless, the proposed testing setup in this work, can be used for SET testing utilizing any of the above-mentioned experiments and to calculate the BER.

Similar to other TPA experiments in this study, laser pulses with 150 fs pulse width and less than 0.9 μm FWHM charge distribution profile in silicon was utilized to induce transients within the devices. The laser energy was continuously monitored throughout the experiment and the average measured laser energy was 2.9 nJ.

The micrograph of the fabricated circuit is shown in Figure 132. See Figure 130. b for the block diagram of the circuit. The generated RF power at the output of the transmitter can be adjusted by adjusting the bias current of the RF VCO. This is required to prevent the saturation of the receiver. A summary of the measured results of the standalone radar receiver without the signal sources is shown in Table 8. The designed mmW receiver is wideband with high linearity and high sensitivity (small NF).

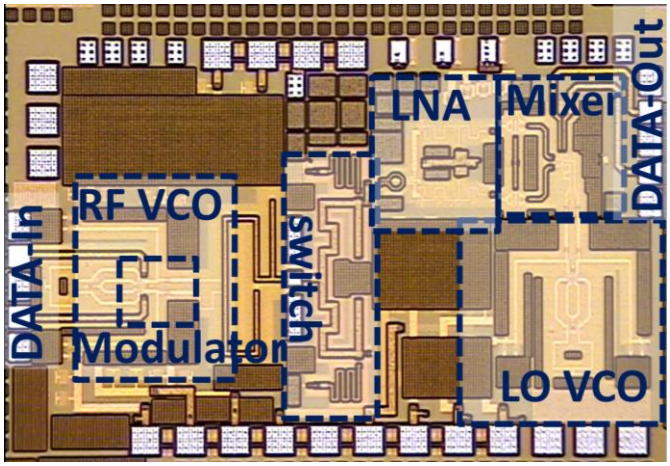

Figure 132. Die photo of the W-band receiver front-end with on-die signal sources and modulation capability.

Table 8. Measured circuit performance.

Measured Performance	
Bandwidth	75-100 GHz
Conversion Gain	6 dB
Noise Figure (NF)	10 dB
Input P1dB	-12 dBm
Power consumption	44.2 mW
Area	2.2×1.4 mm^2
Technology	90 nm IBM-9HP (300 GHz)

Figure 133 shows the schematic diagram of the W-band LNA (see also Figure 130.). The LNA is differential and for simplicity, only a half branch of the circuit is shown in this figure. The main core of the circuit consists of a cascode amplifier stage (Q1 and Q2) with micro-strip matching networks at input and output of the LNA. QB1 and QB2 SiGe HBTs are utilized as a current mirror biasing network. More design details of the circuit can be found in [137].

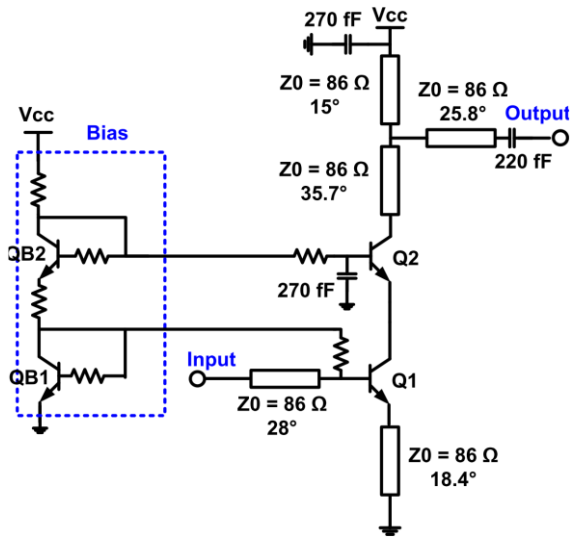

Figure 133. The schematic diagram of the W-band LNA.

A 7 GHz signal tone was applied to the modulator input of the transmitter circuit to emulate the input data stream (see Figure 130.). The receiver is expected to detect, amplify and demodulate and finally recover the same digital data at the output. The output of the receiver was then monitored continuously with a real-time oscilloscope. In all of the measured and simulated data presented in this section, the LO signal (on-die) was always applied to the system for proper operation of the system, unless otherwise stated. Figure 134 shows the snapshot of the transient waveform at the output of the receiver while the QB1 transistor of LNA is being struck by laser pulses. One can see how the 7 GHz data has been received and extracted from the high frequency carrier at the output of the receiver. In addition, the figure shows that a considerable number of data bits are being affected with strong transients induced by laser strikes on the QB1 transistor. Figure 134 also depicts the transient waveform of the receiver output while no data signal is applied

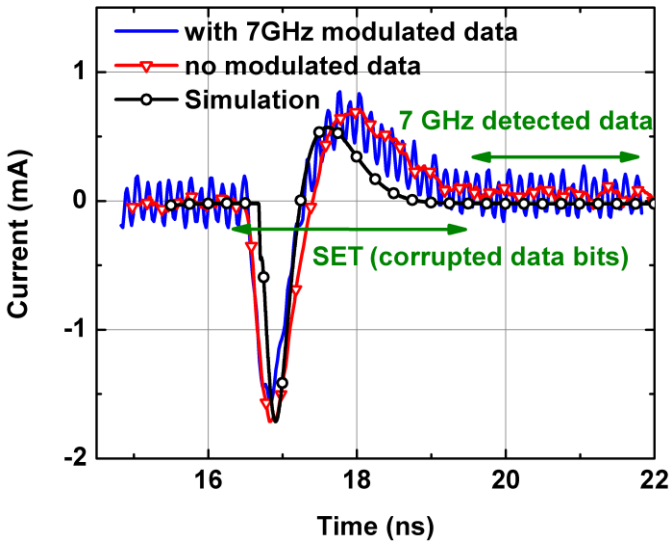

Figure 134. Measured and simulated transient current at the output (IF port) of the receiver for the strike on QB1 SiGe HBT of the LNA with and without applied input data stream.

-to the modulator input. The induced transient in this case follows the transient when the data is present very closely. This is an important observation, since it demonstrates that the induced transient directly sits on top of the received data and corrupts a considerable number of bits in the data stream. This experiment also verifies theoretical analysis in section 5.3.3 demonstrating how SETs propagate throughout the receiver. The transient simulation result is also included in Figure 134 for comparison purposes. A TCAD simulation was performed first on a standalone SiGe HBT and the produced transients were recorded and injected as a current source on QB1 SiGe HBT terminals in the circuit-level simulation. One can observe a close agreement between simulations and measurements. Wire-bond connections as well as cables and oscilloscope loading capacitance were modeled accurately and included in this simulation. Accurate modeling and simulation is particularly important, since it allows the designers to predict and simulate the SET effects on complicated circuit structures, thus allowing designers to add appropriate hardening techniques to mitigate these effects.

It is instructive to note that the shape of the SET response of the circuit is mostly governed by the impulse response of the passive networks present in the circuit, as long as the generated transient from the transistors is short in duration. It is also worth mentioning that since the LO period is much shorter than the produced transient in the circuit, the SET response of the circuit is essentially independent of the strike instant. This can be understood by considering the mixer as a sampling device which is periodically sampling the transient waveform [1]. This observation was verified by collecting the output data of 100 different laser strikes. Figure 135 shows the simulation result of the produced transient at the output of the receiver upon striking the QB1 SiGe HBT, with and without considering the supply wire-bond model. Compared to Figure 134, one can observe the significant effect of the wire-bonds. Although the wire bonds were bypassed with relatively large capacitors inside the chip which is more than enough to bypass the supply node at W-band, (17 pF in this design), the presence of this LPF at this node, increase the duration of the transient significantly. By inspecting Figure 133, one can see that part of the transient present at the supply node as a result of wire-bond effect will appear directly at the output of the LNA, which serves as the input of the down-conversion mixer. This transient signal which has been expanded by the effect of wire-bond as a low-pass filter, is then amplified by the down-conversion mixer to produce a much larger transient at the output of the receiver.

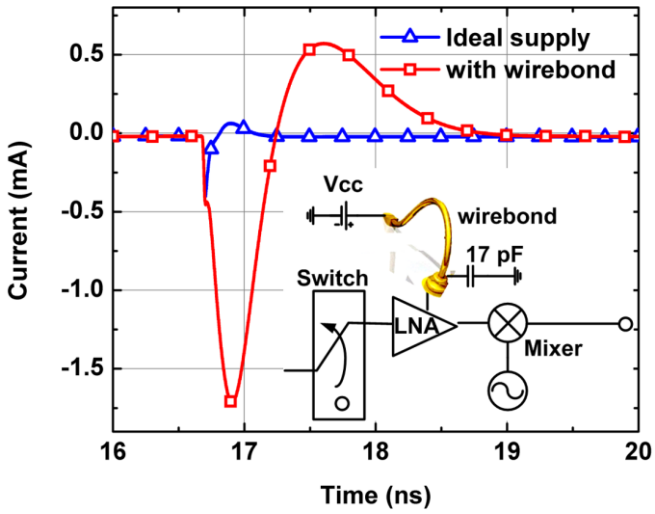

Figure 135. Transient simulation at the output of the radar receiver with and without the supply wire bond.

Figure 136 shows the snapshot of the produced transient current at the output of the receiver for a strike on the Q1 SiGe HBT of the LNA (see Figure 133). Similar to the previous experiment, a 7 GHz tone was fed to the input of the modulator to serve as the digital input signal. Considerable transient current is produced and propagated to the output of the receiver, resulting in several corrupted data bits. In addition, the produced transient without applied modulation data was also captured, and is shown in Figure 136. This data also confirms that the SET sits on top of the digital data with the exact same shape and corrupts the received data. Furthermore, this figure also includes the SET simulation data, using combined device and circuit level simulation explained earlier in this chapter. These simulations closely follow the experimental data.

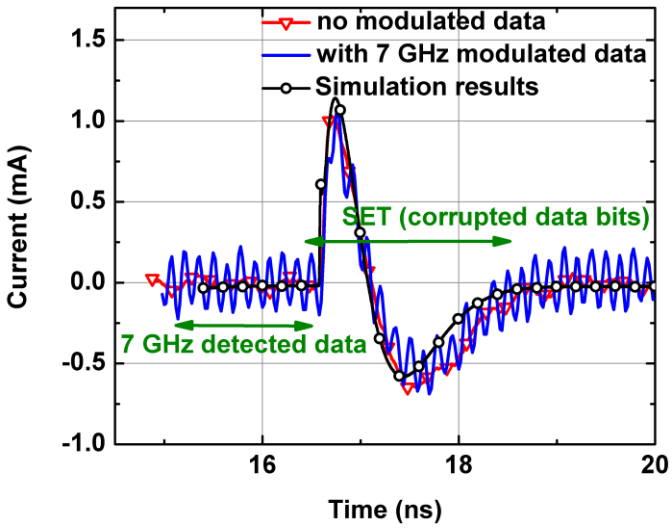

Figure 136. Measured and simulated transient current measured at the output (IF port) of the receiver for the strike on Q1 SiGe HBT of the LNA with and without applied data stream.

Since the emitter terminal of the cascode device was not connected to GND, to capture the relevant terminal transient currents accurately, the entire cascode configuration was simulated in TCAD device-simulator instead of standalone device. The resultant data from cascode terminals was recorded to use in circuit simulations in ADS. Figure 137 shows the measured and simulated results at the output of the receiver for the laser strike on QB2 device. A close agreement between the simulation and measurement results can be observed once again.

In section 5.3, SETs in the down-conversion mixer were investigated; however, no RF and LO signals were applied to the circuit during TPA laser strikes. There it was shown analytically (and supported with TCAD simulations) that the SET propagation to the output of the mmW mixer is independent of the applied LO signal. In the present study, the results of the TPA laser study on the circuit while both LO and RF signals are applied, both confirm and extend the former analysis. In addition, it shows how the induced-

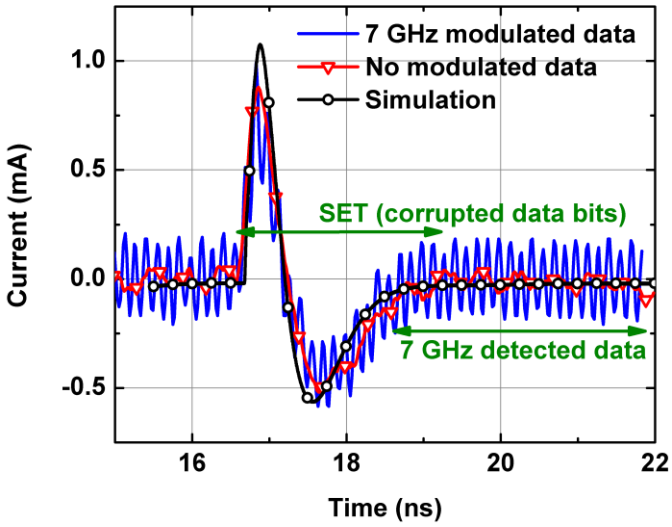

Figure 137. Measured and simulated transient current at the output (IF port) of the receiver for the strike on QB2 cascode SiGe HBT of the LNA with and without applied data stream.

-short transient pulses in mmW receiver circuits are propagated through the receiver chain, are expanded by passing through low-pass filters present at supply nodes and IF port of the receiver and ultimately corrupt multiple data bits. The schematic of the down-conversion mixer can be found in Figure 91 at section 5.3.2.

It was shown in CHAPTER 5 that double-balanced differential mixer is an SET tolerant toplology to eliminate the SETs coming from the stages preceeding the mixer. The generated SET from the circuit components proceeding this mixer toplogy appears as a common-mode transient at differential outputs of the circuit, and can effetively be eliminated if the mixer was designed with high enough linearity. Similar conclusion have been reported in [138] for differential balanced toplogy. To understand this, one can easily see from Figure 91 that any SET coming from Q1 SiGe HBT can find a symmetric path to both differential outputs of the mixer while switch transistors are switching with LO frequency (interested readers are referred to [1]).

The presence of large common-mode transient at differential outputs of the mixer can possibly saturate the mixer and the following IF amplifier, and therefore high linearity is a key feature for the mixer as one of the main SET hardening considerations

Figure 138 shows the measured transient currents at the output of the receiver for a laser strike on Q1 SiGe HBT of the mixer when the LO signal was applied to the mixer compared with the case when the LO signal was turned OFF. No digital input was applied to the circuit to enable clear comparisons. The transient waveform at the output of the receiver is essentially the same regardless of the applied LO signal. A smaller SET peak when the high-power LO is applied can be understood by considering the reduced gain of the mixer due to saturation of the switch transistors with large LO swing. This observation confirms the previous theoretical analysis conducted in section 5.3.3, which showed that SETs longer than twice of the LO period are propagated to the output of the down-conversion mixer in a same shape regardless of the applied LO signal.

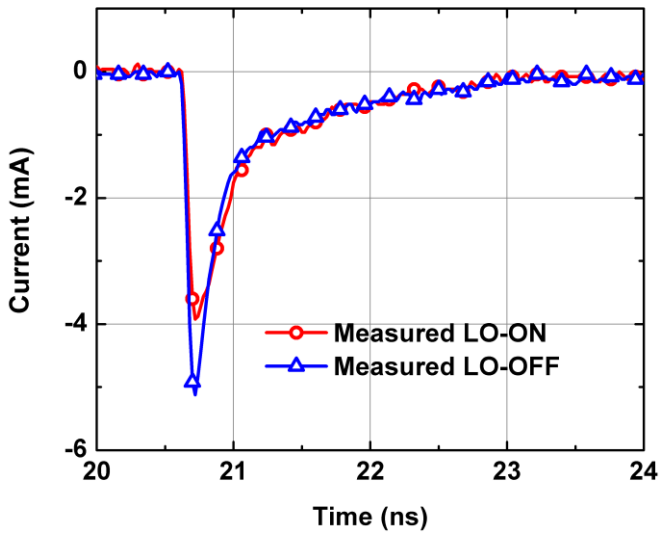

Figure 138. Measured transient current at the output of the receiver with and without LO signal for the strike on Q1 SiGe HBT.

Finally, Figure 139 shows the transient waveform while Q3 SiGe HBT (switch transistor) is being struck. Similar to previous experiments, a 7 GHz input data signal was applied to the transmitter input and demodulated and recovered with the receiver front-end. Simulation follow the experimental data closely, once again verifying the accuracy of the models and simulation approach in the present work.

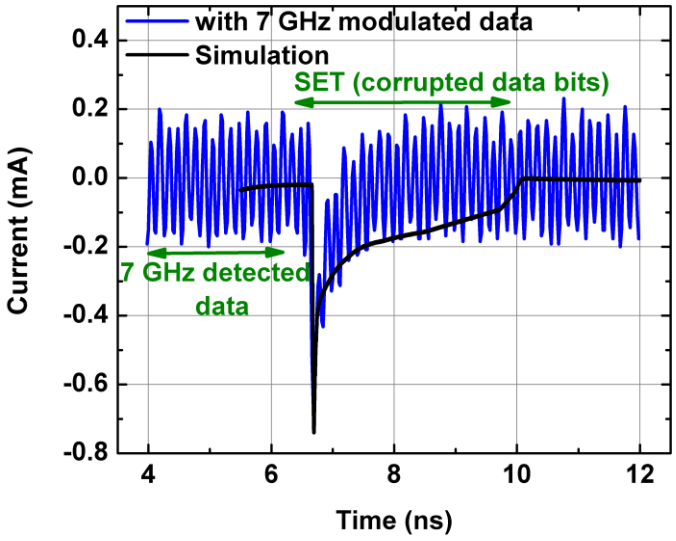

Figure 139. Measured and simulated transient current at the output of the receiver for the strike on one of switch SiGe HBTs (Q3-Q6).

6.5 Summary

SETs in a fully integrated mmW radar receiver were investigated for the first time. The mmW radar front-end was designed and fully implemented in advanced 90 nm SiGe process (GlobalFoundries SiGe 9HP). A technique was proposed, implemented and demonstrated experimentally which allows the SET investigation of high frequency transceivers. A TPA laser experiment was conducted to investigate the SET sensitivity of various circuit blocks in the receiver. It was shown that SETs propagate in the high

frequency receiver chain independent of the applied LO and RF signals when the generated SET is at least as twice as the period of the LO signal. Accurate device and circuit level simulations and modeling were conducted with close agreement with measurement results.

6.6 Radiation-Hardened mmW Receiver

In section 5.3, it was shown that double balanced down-conversion mixer can effectively suppress the SET of g_m transistors (see Figure 91). This means that any SET coming from the proceeding stages of the mixer to the g_m stage can also be suppressed. Block diagram, of the simplified receiver front-end is shown in Figure 140. RF and LO paths are highlighted in this diagram. Similarly, it can be shown that any SET coming from these two paths can effectively be suppressed while passing through double-balanced mixer. In other words, the SET coming from LO and RF paths appears as common mode signal for double balanced mixer and is effectively suppressed in balanced outputs of the mixer. However, it is important to assure that large SET transient which appears as common signal, will not saturate the succeeding stages. In other words, the down-conversion mixer should possess a high linearity to effectively reject the common mode SET without saturation.

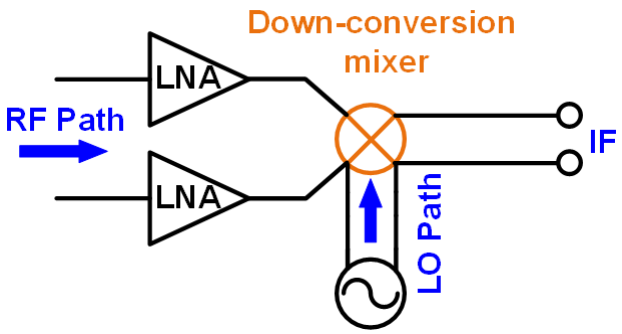

Figure 140. Block diagram of the balanced RF receiver with double balanced down-conversion mixer.

It was also shown that the resultant SETs from an ion strike on switch transistors cannot be suppressed in similar way and in fact appears as pseudo differential signal which increases the SET amplitude. To increase the tolerance of the receiver to strikes on switch

transistors, a passive double balanced mixer is proposed. Switch transistors in passive mixer is not biased thus the produced SET is considerably smaller compared to actively biased transistors. The schematic of the passive mixer is shown in Figure 141. Switch transistors are not biased in this configuration and de-coupled from the g_m stage. The gm transistors however, are biased to provide some conversion gain and minimize the conversion loss of the entire passive mixer. The mmW receiver front-end described in section 6.2 was upgraded to a balanced architecture with a passive double balanced mixer. The die micrograph of the entire receiver front-end including on-chip signal sources and modulators is shown in Figure 142. TPA laser experiment and heavy ion exposure will be conducted as a future work to study the radiation tolerance on the new receiver circuit.

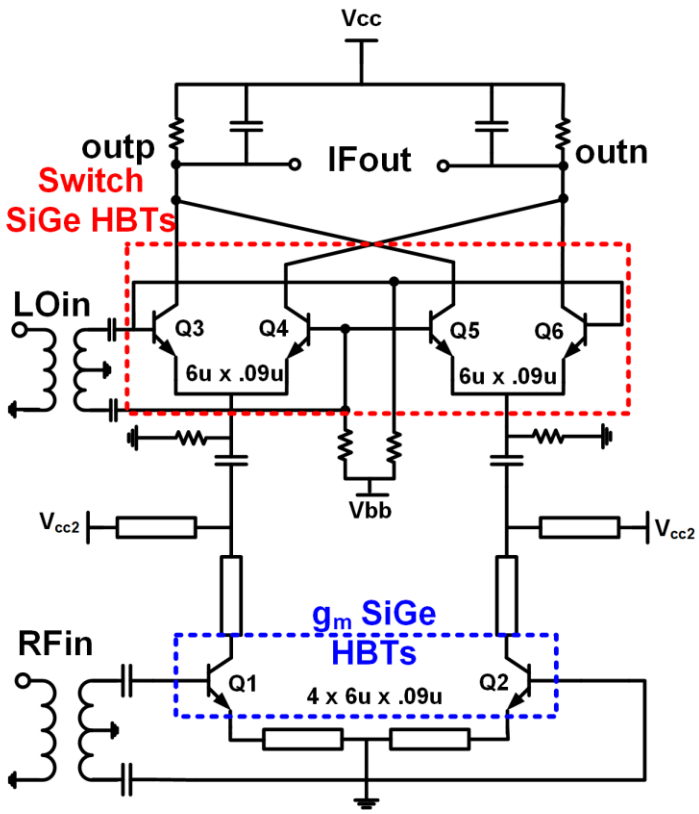

Figure 141. Schematic diagram of the passive down-conversion mixer.

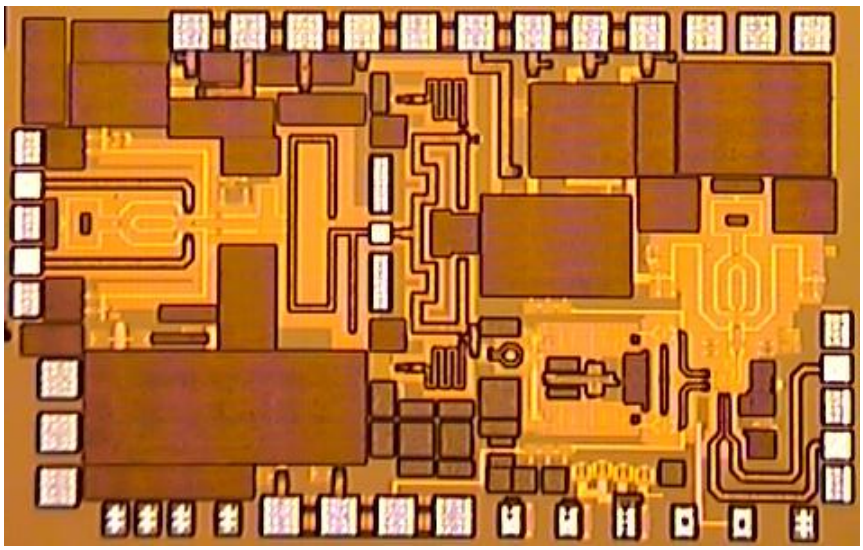

Figure 142. Die micrograph of the radiation-hardened mmW receiver.

CHAPTER 7. CONCLUSION

7.1 Summary of Contributions

The work in the present thesis was focused on developing high frequency millimeter-wave and Terahertz integrated circuits for space applications. Given the limitations of the speed of the current technology at Terahertz frequencies, novel techniques were developed and demonstrated experimentally to realize fully integrated transceivers which include fully phase-locked signal generation circuitries as well as on-die antennas. The reported circuits in this work were among the early realizations of Terahertz circuits in silicon technology and often achieved record performance metrics by utilizing novel circuit techniques and architectures. In addition, the effects of radiation intensive environments were studied for the first time on RF receiver front-end at millimeter-wave frequencies. Several experiments, modeling, analyses and simulations were conducted to understand the effects of single-event transients on RF circuit and systems.

The specific contributions include:

1. Developing several signal sources and phase-locked-loop (PLL) circuits at millimeter-wave and Terahertz frequencies with novel techniques to improve the performance and set the performance record among silicon based implementations.
2. Developing novel phase locking scheme to synchronize free running signal sources together with wide bandwidth and strong coupling conditions.

3. Developing fully integrated, fully phase-locked transmitter arrays including on-chip PLL and on-die antennas with novel techniques to improve the transmitter power at THz frequencies.
4. Developing several fully integrated transceiver modules with on-chip PLL and on-die antennas at mmW and THz frequencies utilizing novel techniques to improve the sensitivity of receiver and output power of the transmitters.
5. First experimental study, theoretical analysis, modeling and simulations of the radiation effects on millimeter-wave RF components and receiver front-end.

7.2 Future Work

Research on millimeter-wave and Terahertz frequency range has gain lots of attentions in recent years and several research teams across the world are actively involved in developing these types of systems. In addition, there is a growing interest in utilizing mmW and THz circuits for scientific explorations such as space applications. Integrated Radiometers and Radars at mmW frequencies are currently being developed for use in CubeSats.

The results from the current study demonstrated the possibility of the implementation of complicated Terahertz circuits utilizing the current technologies. In addition, operation of mmW circuits were investigated in radiation intensive environments. The research presented in this work, can be extended in the following directions:

1. Developing novel modulator architectures for high data rate communications. One of the main advantageous of mmW and Terahertz frequencies come from the available wide bandwidth at these frequencies. Possibility of a wireless link at these

frequencies was successfully demonstrated by realizing several T/R modules in this study. With inclusion of wideband modulation schemes, high data rate communication link can be realized and demonstrated.

2. Fully phase-locked transmitters were implemented, this work can be further extended by adding electrical phase steering capability to create phased arrays.
3. A couple of novel circuit design techniques were demonstrated in the present work to improve the sensitivity of receivers and output power of the transmitter. There is still plenty of room for creative circuit design techniques to improve the sensitivity of receivers, RF power of the transmitters and novel on-chip antenna concepts for better layout and wideband operation.
4. Radiation effects on RF systems were studied and understood in this work, novel radiation hardening techniques can now be developed to mitigate the detrimental effects of single-event transients on these systems by utilizing circuit design techniques.
5. TPA laser experiments were conducted as an experimental tool for electron-hole generation within the devices. Heavy ion exposure is the next step to test these systems and validate the findings in the present work as well as radiation hardening schemes.
6. Correlation of TPA laser beams with heavy ion exposure has already been started in our team at device level. Further experiments on circuit level can be useful for improving the developed models in this work for more realistic scenarios.

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